A6985F

38 V, 500 mA synchronous step-down switching regulator with 30 µA quiescent current

Datasheet - production data

HTSSOP16 (R_{TH} = 40 °C/W)

Features

- AECQ100 qualification
- 0.5 A DC output current
- 4 V to 38 V operating input voltage
- Low consumption mode or low noise mode
- 30 µA I_Q at light-load (LCM V_{OUT} = 3.3 V)
- 8 µA $I_{Q\text{-}SHTDWN}$
- Fixed output voltage (3.3 V and 5 V) or adjustable from 0.85 V to V_{IN}
- Adjustable f_{SW} (250 kHz - 2 MHz)
- Embedded output voltage supervisor
- Synchronization
- Adjustable soft-start time
- Internal current limiting
- Overvoltage protection
- Output voltage sequencing
- Peak current mode architecture
- $R_{DSON\ HS}$ = 360 mΩ, $R_{DSON\ LS}$ = 150 mΩ
- Thermal shutdown

Applications

- Designed for automotive systems
- Battery powered applications
- Car body applications (LCM)
- Car audio and low noise applications (LNM)

Description

The A6985F automotive grade device is a step-down monolithic switching regulator able to deliver up to 0.5 A DC. The output voltage adjustability ranges from 0.85V to VIN. The 100% duty cycle capability and the wide input voltage range meet the cold crank and load dump specifications for automotive systems. The “Low Consumption Mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at light-load with controlled output voltage ripple. The “Low Noise Mode” (LNM) makes the switching frequency constant and minimizes the output voltage ripple overload current range, meeting the low noise application specification like car audio. The output voltage supervisor manages the reset phase for any digital load (µC, FPGA). The RST open collector output can also implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact. Pulse by pulse current sensing on both power elements implements an effective constant current protection.

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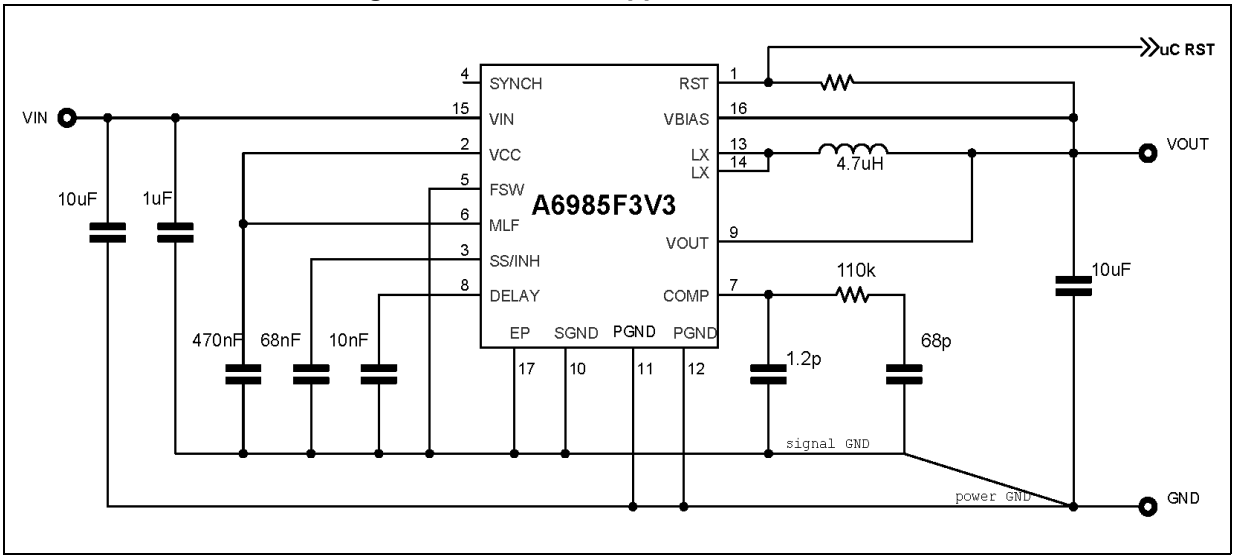
1 Application schematic

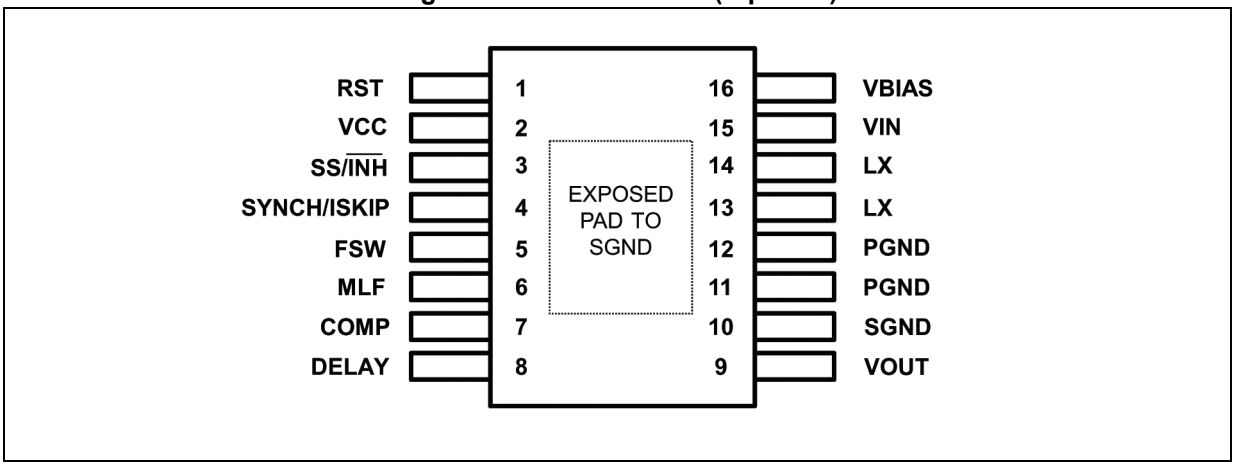
Figure 1. A6985F3V3 application schematic



2 Pin settings

2.1 Pin connection

Figure 2. Pin connection (top view)



2.2 Pin description

Table 1. Pin description

No.	Pin	Description
1	RST	The RST open collector output is driven low when the output voltage is out of regulation. The RST is released after an adjustable time DELAY once the output voltage is over the active delay threshold.
2	VCC	Connect a ceramic capacitor (≥ 470 nF) to filter internal voltage reference. This pin supplies the embedded analog circuitry.
3	SS/$\overline{\text{INH}}$	An open collector stage can disable the device clamping this pin to GND ($\overline{\text{INH}}$ mode). An internal current generator (2 µA typ.) charges the external capacitor to implement the soft-start.
4	SYNCH/ ISKP	The pin features Master / Slave synchronization in LNM (see *Section 7.5 on page 48*) and skip current level selection in LCM (see *Section 5.5.2 on page 27*).
5	FSW	A pull up resistor (E24 series only) to VCC or pull down to GND selects the switching frequency. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
6	MLF	A pull up resistor (E24 series only) to VCC or pull down to GND selects the low noise mode/low consumption mode and the active RST threshold. Pinstrapping is active only before the soft-start phase to minimize the IC consumption.
7	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
8	DELAY	An external capacitor connected at this pin sets the time DELAY to assert the rising edge of the RST o.c. after the output voltage is over the reset threshold. If this pin is left floating, RST is like a Power Good.
9	VOUT	Output voltage sensing
10	SGND	Signal GND

Table 1. Pin description (continued)

No.	Pin	Description
11	PGND	Power GND
12	PGND	Power GND
13	LX	Switching node
14	LX	Switching node
15	VIN	DC input voltage
16	V_{BIAS}	Typically connected to the regulated output voltage. An external voltage reference can be used to supply part of the analog circuitry to increase the efficiency at light-load. Connect to GND if not used.
-	E. p.	Exposed pad must be connected to SGND, PGND.

2.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	See *Table 1*	-0.3	40	V
DELAY		-0.3	V_{CC} + 0.3	V
PGND		SGND - 0.3	SGND + 0.3	V
SGND				V
V_{CC}		-0.3	(V_{IN} + 0.3) or (max. 4)	V
SS / $\overline{INH}$		-0.3	V_{IN} + 0.3	V
MLF		-0.3	V_{CC} + 0.3	V
COMP		-0.3	V_{CC} + 0.3	V
VOUT		-0.3	10	V
FSW		-0.3	V_{CC} + 0.3	V
SYNCH		-0.3	V_{IN} + 0.3	V
V_{BIAS}		-0.3	(V_{IN} + 0.3) or (max. 6)	V
RST		-0.3	V_{IN} + 0.3	V
LX		-0.3	V_{IN} + 0.3	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range		-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 sec.)		260	°C
I_{HS}, I_{LS}	High-side / low-side switch current		2	A

2.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on the STMicroelectronics® demonstration board)	40	C/W
$R_{th\ JC}$	Thermal resistance junction to exposed pad for board design (not suggested to estimate TJ from power losses).	5	C/W

2.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	kV
	MM	200	V
	CDM	500	V

3 Electrical characteristics

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range			4		38	V
V_{INH}	V_{CC} UVLO rising threshold			2.7		3.5	
V_{INL}	V_{CC} UVLO falling threshold			2.4		3.5	
I_{PK}	Peak current limit	Duty cycle < 20%		0.8			A
		Duty cycle = 100% closed loop operation		0.65			
I_{VY}	Valley current limit			0.9			
I_{SKIP}	Skip current limit	LCM, V_{SYNCH} = GND	(1)	0.15	0.35	0.5	
		LCM, V_{SYNCH} = VCC	(2)		0.1		
I_{VY_SNK}	Reverse current limit	LNM or V_{OUT} overvoltage		0.5	1	2	
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 0.5 A			0.36	0.72	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 0.5 A			0.15	0.30	
f_{SW}	Selected switching frequency	FSW pinstrapping before SS		See *Table 6: f_{SW} selection*			
I_{FSW}	FSW biasing current	SS ended			0	500	nA
LCM/LNM	Low noise mode / Low consumption mode selection	MLF pinstrapping before SS		See *Table 7 on page 12*, *Table 8 on page 13*, *Table 9 on page 13*			
I_{MLF}	MLF biasing current	SS ended			0	500	nA
D	Duty cycle		(2)	0		100	%
$T_{ON\ MIN}$	Minimum On time				80		ns
VCC regulator							
V_{CC}	LDO output voltage	V_{BIAS} = GND (no switchover)		2.9	3.3	3.6	V
		V_{BIAS} = 5 V (switchover)		2.9	3.3	3.6	
SWO	V_{BIAS} threshold (3 V< V_{BIAS} < 5.5 V)	Switch internal supply from V_{IN} to V_{BIAS}		2.85		3.2	
		Switch internal supply from V_{BIAS} to V_{IN}		2.78		3.15	

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	$V_{SS/INH}$ = GND		4	8	15	µA
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	4	10	15	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(3)	35	70	120	
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V		0.5	1.5	5	mA
		LNM - NO SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = GND		2	2.8	6	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(3)	25	50	115	µA
		LNM - SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V		0.5	1.2	5	mA
Soft-start							
V_{INH}	VSS threshold	SS rising		200	460	700	mV
$V_{INH\ HYST}$	VSS hysteresis				100	140	
$I_{SS\ CH}$	C_{SS} charging current	$V_{SS} < V_{INH}$ OR $t < T_{SS\ SETUP}$ OR $V_{EA+} > V_{FB}$	(2)		1		µA
		$t > T_{SS\ SETUP}$ AND $V_{EA+} < V_{FB}$	(2)		4		
$V_{SS\ START}$	Start of internal error amplifier ramp			0.995	1.1	1.150	V
SS_{GAIN}	SS/INH to internal error amplifier gain				3		
Error amplifier							
V_{OUT}	Voltage feedback	3.3 V (A6985F3V3)		3.25	3.3	3.35	V
		5 V (A6985F5V)		4.925	5.0	5.075	
		A6985F		0.841	0.85	0.859	
I_{VOUT}	VOUT biasing current	3.3 V (A6985F3V3)		4	6	8.5	µA
		5 V (A6985F5V)		7.5	10	13.5	
		A6985F			50	500	nA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Note	Min.	Typ.	Max.	Unit
A_V	Error amplifier gain		(2)		100		dB
I_{COMP}	EA output current capability			±6	±12	±25	µA
			(4)	±4			
Inner current loop							
g_{CS}	Current sense transconductance (V_{COMP} to inductor current gain)	I_{PK} = 0.5 A	(2)		1.67		A/V
$V_{PP} \cdot g_{CS}$	Slope compensation		(5)	0.2	0.3	0.4	A
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})			1.15	1.2	1.25	
$V_{OVP\ HYST}$	Overvoltage hysteresis			0.5	2	5	%
Synchronization (fan out: 6 slave devices typ.)							
$f_{SYN\ MIN}$	Synchronization frequency	LNM; f_{SW} = VCC		266.5			kHz
$V_{SYN\ TH}$	SYNCH input threshold	LNM, SYNCH rising		0.70		1.2	V
I_{SYN}	SYNCH pulldown current	LNM, V_{SYN} = 1.2 V			0.7		mA
$V_{SYN\ OUT}$	High level output	LNM, 5 mA sinking load		1.40			V
	Low level output	LNM, 0.7 mA sourcing load				0.6	
Reset							
V_{THR}	Selected RST threshold	MLF pinstrapping before SS		See *Table 7*, *Table 8*, *Table 9*			
$V_{THR\ HYST}$	RST hysteresis		(2)		2		%
V_{RST}	RST open collector output	$V_{IN} > V_{INH}$ AND $V_{FB} < V_{TH}$ 4 mA sinking load				0.4	V
		$2 < V_{IN} < V_{INH}$ 4 mA sinking load				0.8	
Delay							
V_{THD}	RST open collector released as soon as $V_{DELAY} > V_{THD}$	$V_{FB} > V_{THR}$		1.19	1.234	1.258	V
$I_{D\ CH}$	C_{DELAY} charging current	$V_{FB} > V_{THR}$		1	2	3	µA
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature		(2)		165		°C
T_{HYS}	Thermal shutdown hysteresis		(2)		30		

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. Not tested in production.
3. LCM enables SLEEP mode at light-load.
4. T_J = -40°C.
5. Measured at f_{sw} = 250 kHz.

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 6. f_{SW} selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	Tj	f_{SW} min.	f_{SW} typ.	f_{SW} max.	Unit
f_{SW}	0 Ω	NC		225	**250**	275	kHz
	1.8 kΩ	NC	(1)		**285**		
	3.3 kΩ	NC			**330**		
	5.6 kΩ	NC			**380**		
	10 kΩ	NC			**435**		
	NC	0 Ω		450	**500**	550	
	18 kΩ	NC	(1)		**575**		
	33 kΩ	NC			**660**		
	56 kΩ	NC			**755**		
	NC	1.8 kΩ			**870**		
	NC	3.3 kΩ		900	**1000**	1100	
	NC	5.6 kΩ	(1)		**1150**		
	NC	10 kΩ			**1310**		
	NC	18 kΩ			**1500**(2)		
	NC	33 kΩ		1575	**1750**(2)	1925	
	NC	56 kΩ		1800	**2000**(2)	2200	

1. Not tested in production.
2. No synchronization as slave in LNM.

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 7. LNM / LCM selection (A6985F3V3)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	3.008	3.069	3.130	V
	8.2 kΩ	NC		**80%**	2.587	**2.640**	2.693	
	18 kΩ	NC		**87%**	2.814	**2.871**	2.928	
	39 kΩ	NC		**96%**	3.105	**3.168**	3.231	
	NC	0 Ω	**LNM**	**93%**	3.008	3.069	3.130	
	NC	8.2 kΩ		**80%**	2.587	**2.640**	2.693	
	NC	18 kΩ		**87%**	2.814	**2.871**	2.928	
	NC	39 kΩ		**96%**	3.105	**3.168**	3.231	

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 8. LNM / LCM selection (A6985F5V)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	LCM	**93%**	4.557	**4.650**	4.743	V
	8.2 kΩ	NC		**80%**	3.920	**4.000**	4.080	
	18 kΩ	NC		**87%**	4.263	**4.350**	4.437	
	39 kΩ	NC		**96%**	4.704	**4.800**	4.896	
	NC	0 Ω	LNM	**93%**	4.557	**4.650**	4.743	
	NC	8.2 kΩ		**80%**	3.920	**4.000**	4.080	
	NC	18 kΩ		**87%**	4.263	**4.350**	4.437	
	NC	39 kΩ		**96%**	4.704	**4.800**	4.896	

T_J = -40 to 135 °C, V_{IN} = 12 V unless otherwise specified.

Table 9. LNM / LCM selection table (A6985F)

Symbol	R_{VCC} (E24 1%)	R_{GND} (E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	LCM	**93%**	0.779	**0.791**	0.802	V
	8.2 kΩ	NC		**80%**	0.670	**0.680**	0.690	
	18 kΩ	NC		**87%**	0.728	**0.740**	0.751	
	39 kΩ	NC		**96%**	0.804	**0.816**	0.828	
	NC	0 Ω	LNM	**93%**	0.779	**0.791**	0.802	
	NC	8.2 kΩ		**80%**	0.670	**0.680**	0.690	
	NC	18 kΩ		**87%**	0.728	**0.740**	0.751	
	NC	39 kΩ		**96%**	0.804	**0.816**	0.828	

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +135 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +135 °C).

The device operation is guaranteed when the junction temperature is inside the (-40 °C, +150 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+165 °C typ.) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +135 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

5 Functional description

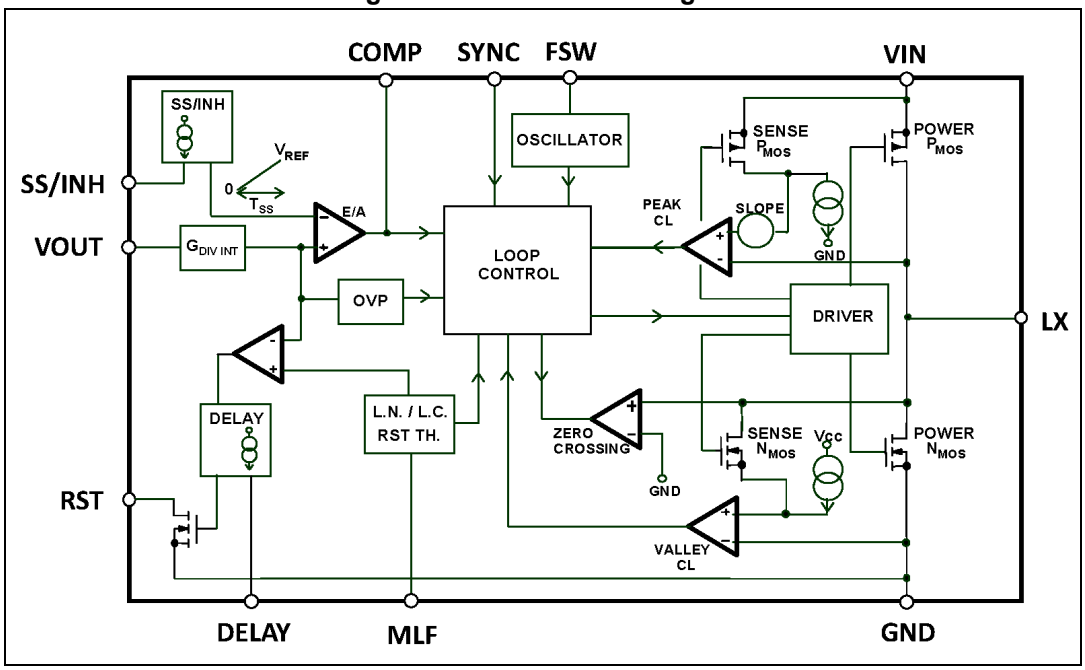
The A6985F device is based on a “peak current mode”, constant frequency control. As a consequence, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load.

The main internal blocks shown in the block diagram in *Figure 3* are:

- Embedded power elements. Thanks to the P-channel MOSFET as high-side switch the device features low dropout operation
- A fully integrated sawtooth oscillator with adjustable frequency
- A transconductance error amplifier
- An internal feedback divider $G_{DIV\ INT}$
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decreases the inrush current at power-up. The SS/$\overline{\text{INH}}$ pin inhibits the device when driven low.
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the V_{BIAS} pin is connected to an external output voltage
- The synchronization circuitry to manage master / slave operation and the synchronization to an external clock
- The current limitation circuit to implement the constant current protection, sensing pulse by pulse high-side / low-side switch current. In case of heavy short-circuit the current protection is fold back to decrease the stress of the external components
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- MLF pin strapping sets the LNM/LCM mode and the thresholds of the RST comparator
- FSW pinstrapping sets the switching frequency
- The RST open collector output

Figure 3. Internal block diagram



5.1 Power supply and voltage reference

The internal regulator block consists of a start-up circuit, the voltage pre-regulator that provides current to all the blocks and the bandgap voltage reference. The starter supplies the startup current when the input voltage goes high and the device is enabled (SS/INH pin over the inhibits threshold).

The pre-regulator block supplies the bandgap cell and the rest of the circuitry with a regulated voltage that has a very low supply voltage noise sensitivity.

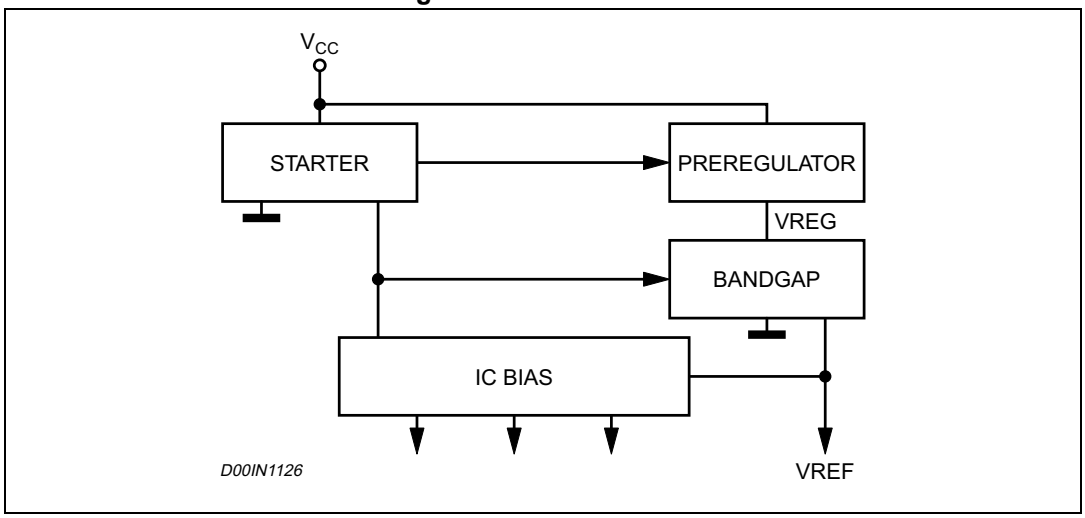
Switchover feature

The switchover scheme of the pre-regulator block features to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS} < 5.5 V is typically connected to the regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}. (please refer to *Section 5.6: Switchover feature on page 31*).

5.2 Voltages monitor

An internal block continuously senses the V_{CC}, V_{BIAS} and V_{BG}. If the monitored voltages are good, the regulator starts operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



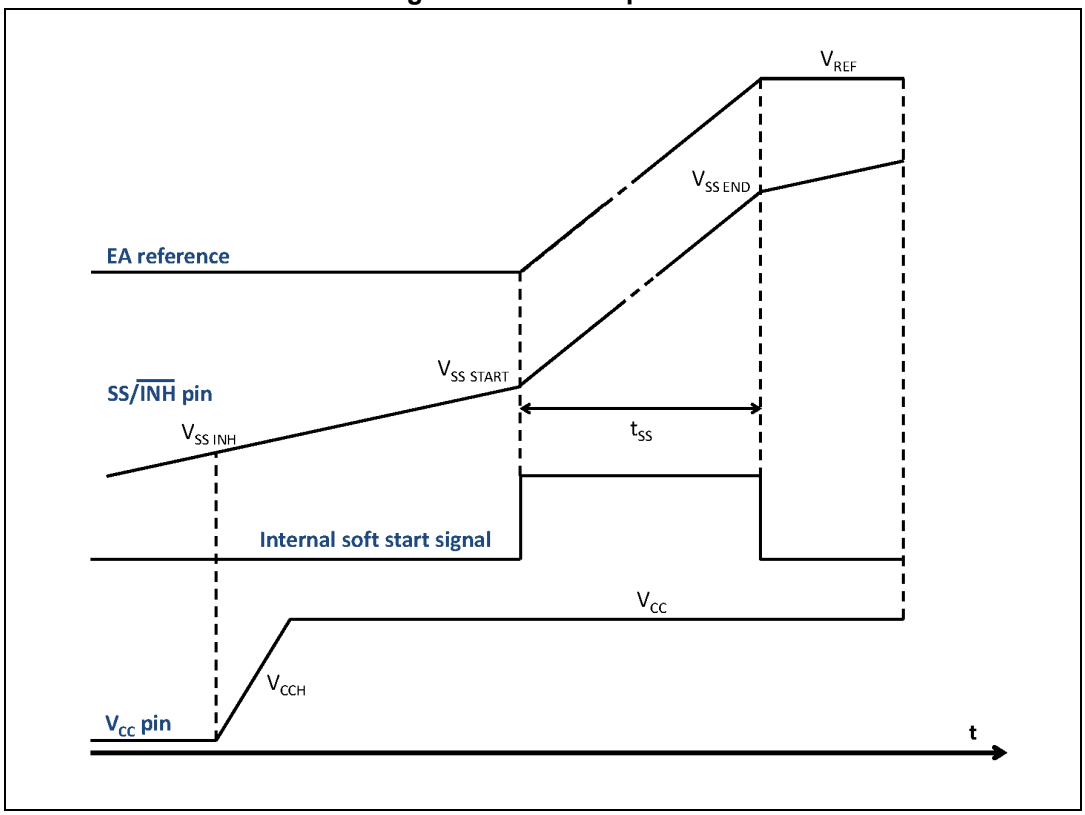
5.3 Soft-start and inhibit

The soft-start and inhibit features are multiplexed on the same pin. An internal current source charges the external soft-start capacitor to implement a voltage ramp on the SS/INH pin. The device is inhibited as long as the SS/INH pin voltage is lower than the V_{INH} threshold and the soft-start takes place when SS/INH pin crosses $V_{SS\ START}$. (See *Figure 5*).

The internal current generator sources 1 µA typ. current when the voltage of the VCC pin crosses the UVLO threshold. The current increases to 4 µA typ. as soon as the SS/INH voltage is higher than the V_{INH} threshold. This feature helps to decrease the current consumption in inhibit mode. An external open collector can be used to set the inhibit operation clamping the SS/INH voltage below V_{INH} threshold.

The startup feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The ramp implemented on the reference of the error amplifier has a gain three times higher (SS_{GAIN}) than the external ramp present at SS/INH pin.

Figure 5. Soft-start phase



The C_{SS} is dimensioned accordingly with *Equation 1*:

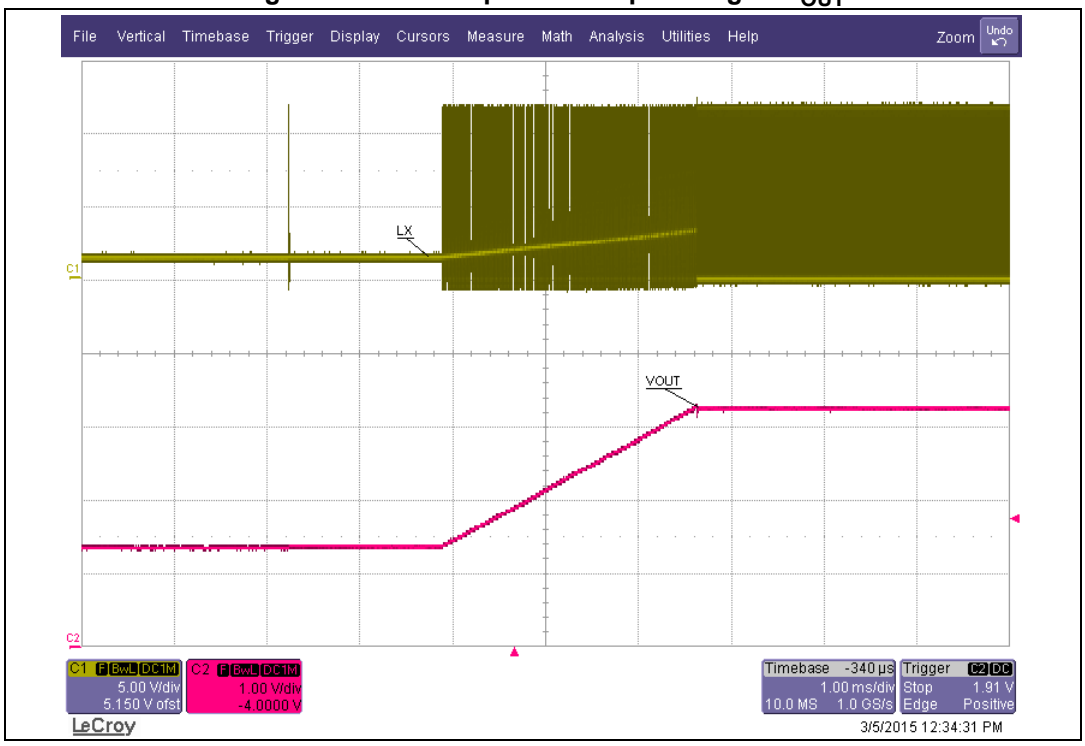
Equation 1

$$C_{SS} = SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where T_{SS} is the soft-start time, $I_{SS\ CH}$ the charging current and V_{FB} the reference of the error amplifier.

The soft-start block supports the precharged output capacitor.

Figure 6. Soft-start phase with precharged C_{OUT}



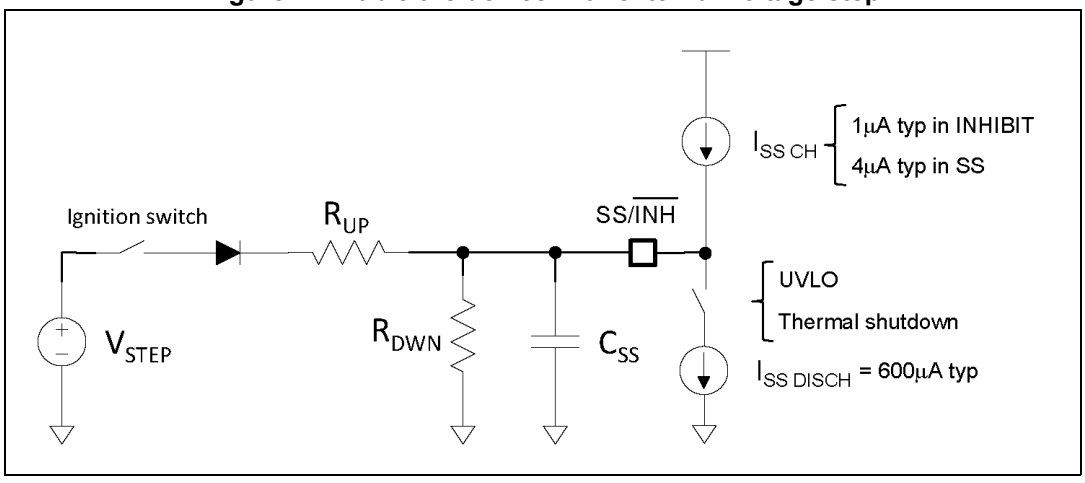
During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- The device is driven in $\overline{INH}$ mode

The soft-start capacitor is discharged with a 0.6 mA typ. current capability for 1 msec time max. For complete and proper capacitor discharge in case of fault condition, a maximum C_{SS} = 67 nF value is suggested.

The application example in *Figure 7* shows how to enable the A6985F and perform the soft-start phase driven by an external voltage step, for example the signal from the ignition switch in automotive applications.

Figure 7. Enable the device with external voltage step



The maximum capacitor value has to be limited to guarantee the device can discharge it in case of thermal shutdown and UVLO events (see *Section 5.3.1*), so restart the switching activity ramping the error amplifier reference voltage.

Equation 2

$$C_{SS} < \frac{-1\ \text{msec}}{R_{SS\_EQ} \cdot \ln\left(1 - \frac{V_{SS\_FINAL} - 0.9\ V}{600\ \mu A - R_{SS\_EQ}}\right)}$$

where:

Equation 3

$$R_{SS\_EQ} = \frac{R_{UP} \cdot R_{DWN}}{R_{UP} + R_{DWN}} \qquad V_{SS\_FINAL} = (V_{STEP} - V_{DIODE}) \cdot \frac{R_{DWN}}{R_{UP} + R_{DWN}}$$

The optional diode prevents to disable the device if the external source drops to ground.

R_{UP} value is selected in order to make the capacitor charge at first approximation independent from the internal current generator (4 µA typ. current capability, see *Table 5 on page 9*), so:

Equation 4

$$\frac{V_{STEP} - V_{DIODE} - V_{SS\ END}}{R_{UP}} \gg I_{SS\ CHARGE} \equiv 4\ \mu A$$

where:

Equation 5

$$V_{SS\ END} = V_{SS\ START} + \frac{V_{FB}}{SS_{GAIN}}$$

represents the SS/$\overline{\text{INH}}$ voltage correspondent to the end of the ramp on the error amplifier (see *Figure 5*); refer to *Table 5* for $V_{SS\ START}$, V_{FB} and SS_{GAIN} parameters.

As a consequence the voltage across the soft-start capacitor can be written as:

Equation 6

$$v_{SS}(t) = V_{SS\_FINAL} \cdot \frac{1}{1 - e^{-\frac{t}{C_{SS} \cdot R_{SS\_EQ}}}}$$

R_{SS_DOWN} is selected to guarantee the device stays in inhibit mode when the internal generator sources 1 µA typ. out of the SS/INH pin and V_{STEP} is not present:

Equation 7

$$R_{DWN} \cdot I_{SS\ INHIBIT} \equiv R_{DWN} \cdot 1\ \mu A \ll V_{INH} \equiv 200\ mV$$

so:

Equation 8

$$R_{DWN} < 100\ k\Omega$$

R_{UP} and R_{DWN} are selected to guarantee:

Equation 9

$$V_{SS\_FINAL} \cong 2\ V > V_{SS\_END}$$

The time to ramp the internal voltage reference can be calculated from *Equation 10*:

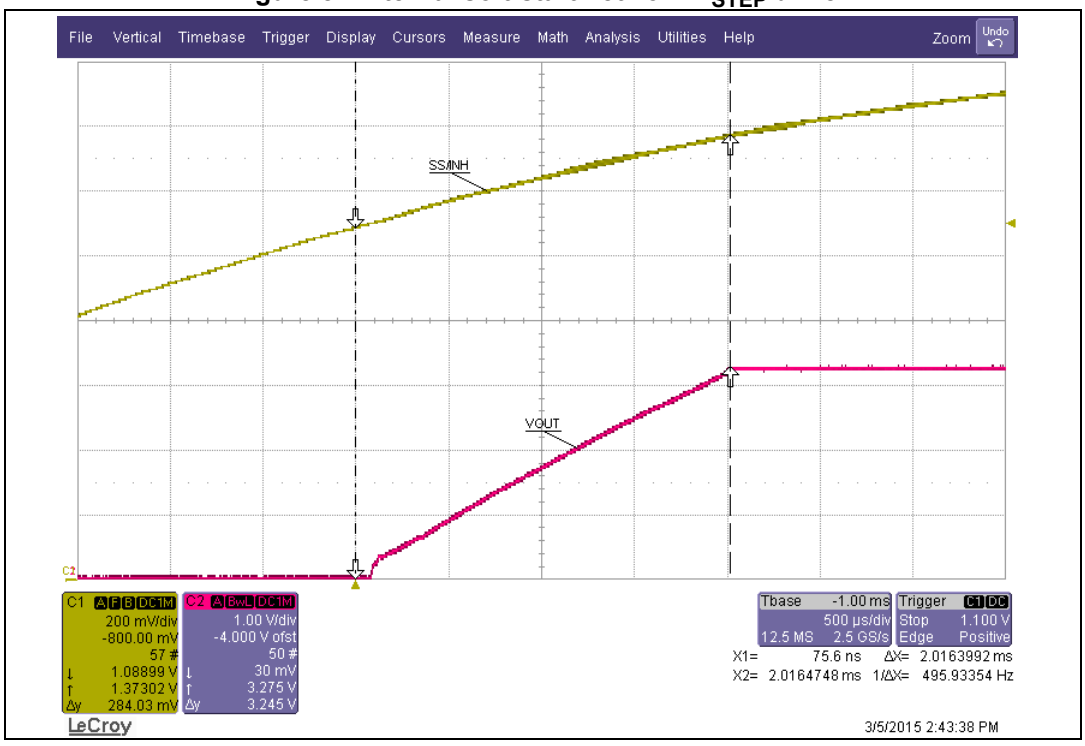
Equation 10

$$T_{SS} = C_{SS} \cdot R_{SS\_EQ} \cdot \ln\left(\frac{V_{SS\_FINAL} - V_{SS\ START}}{V_{SS\_FINAL} - V_{SS\ END}}\right)$$

that is the equivalent soft-start time to ramp the output voltage.

Figure 8 shows the soft-start phase with the following component selection: R_{UP} = 180 kΩ, R_{DWN} = 33 kΩ, C_{SS} = 200 nF, the 1N4148 is a small signal diode and V_{STEP} = 13 V.

Figure 8. External soft-start network V_{STEP} driven



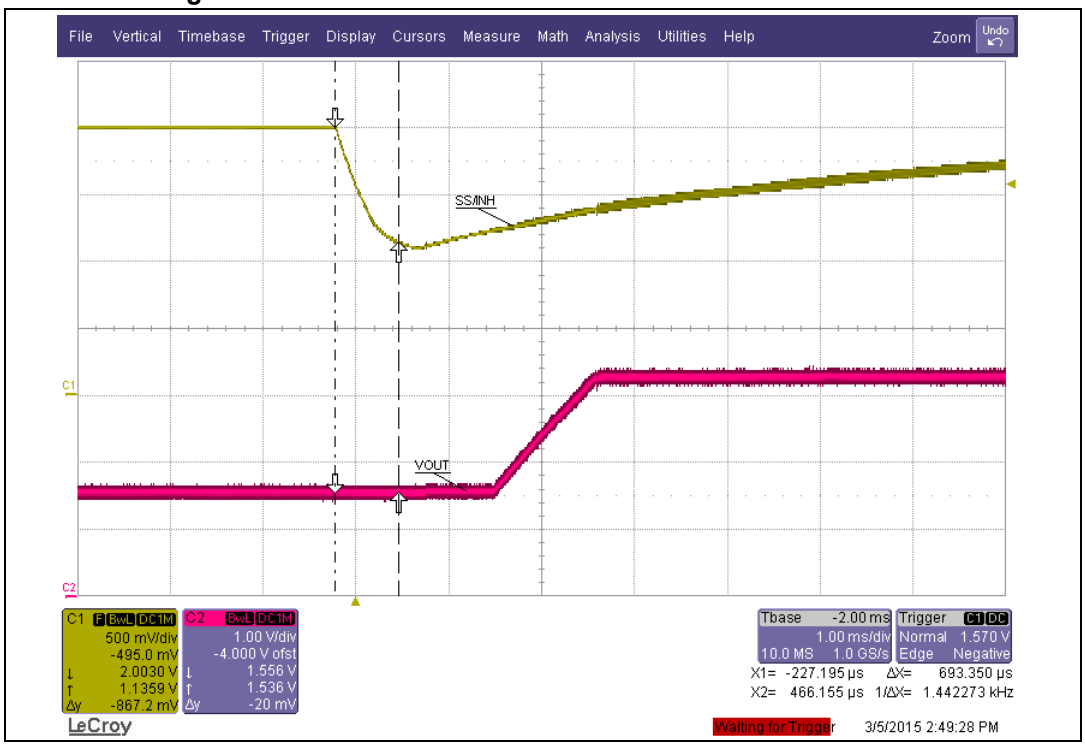
The circuit in *Figure 7* introduces a time delay between V_{STEP} and the switching activity that can be calculated as:

Equation 11

$$T_{SS\ DELAY} = C_{SS} \cdot R_{SS\_EQ} \cdot \ln\left(\frac{V_{SS\_FINAL}}{V_{SS\_FINAL} - V_{SS\ START}}\right)$$

Figure 9 shows how the device discharges the soft-start capacitor after an UVLO or thermal shutdown event in order to restart the switching activity ramping the error amplifier reference voltage.

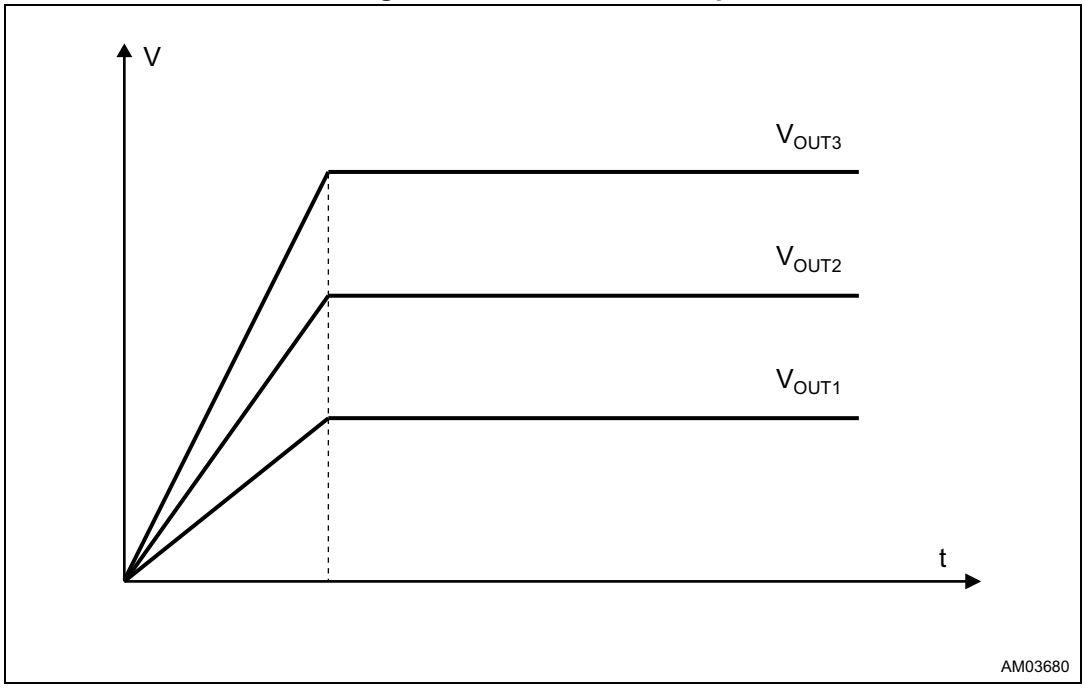
Figure 9. External soft-start after UVLO or thermal shutdown



5.3.1 Ratiometric startup

The ratiometric startup is implemented sharing the same soft-start capacitor for a set of the A6985F devices.

Figure 10. Ratiometric startup



As a consequence all the internal current generators charge in parallel the external capacitor. The capacitor value is dimensioned accordingly with *Equation 12*:

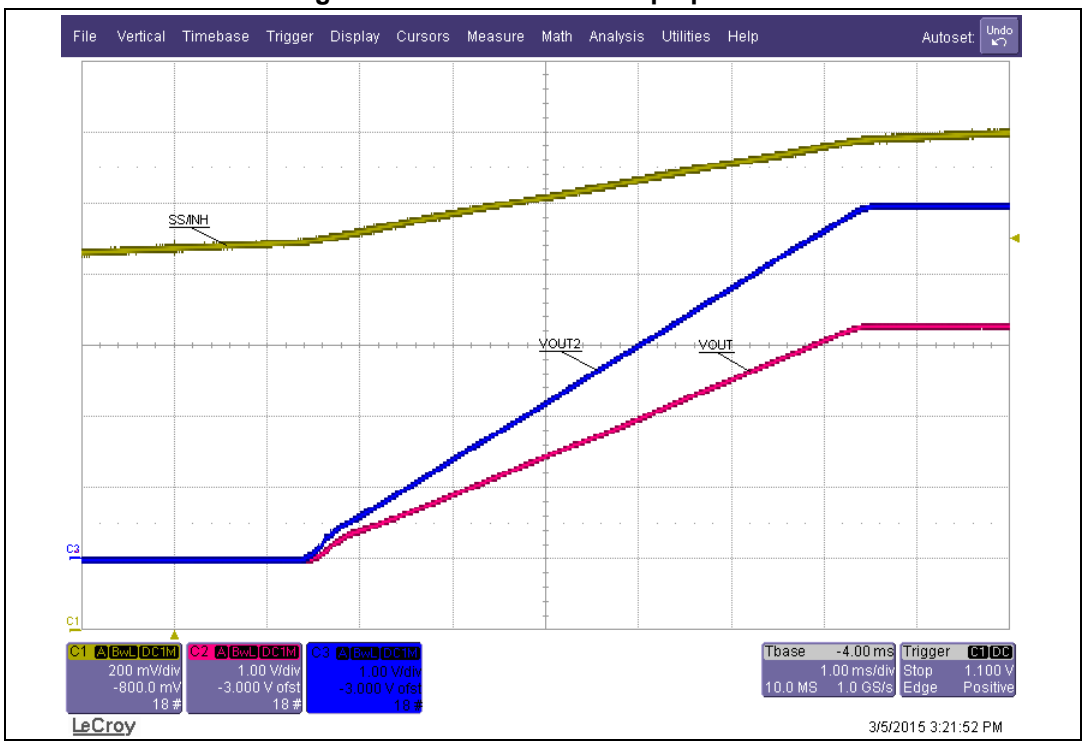
Equation 12

$$C_{SS} = n_{A6985F} \bullet SS_{GAIN} \bullet \frac{I_{SSCH} \bullet T_{SS}}{V_{FB}} = n_{A6985F} \bullet 3 \bullet \frac{4\mu A \bullet T_{SS}}{0.85V}$$

where n_{A6985F} represents the number of devices connected in parallel.

For better tracking of the different output voltages the synchronization of the set of regulators is suggested.

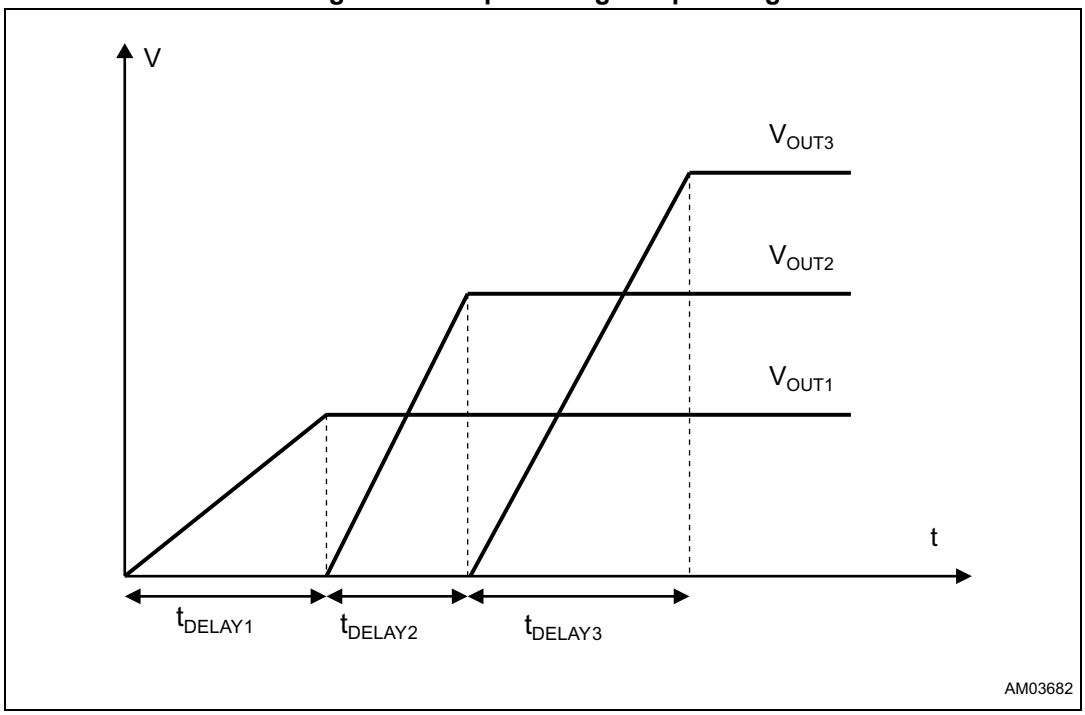
Figure 11. Ratiometric startup operation



5.3.2 Output voltage sequencing

The A6985F device implements sequencing connecting the RST pin of the master device to the SS/INH of the slave. The slave is inhibited as long as the master output voltage is outside regulation so implementing the sequencing (see *Figure 12*).

Figure 12. Output voltage sequencing



High flexibility is achieved thanks to the programmable RST thresholds (see *Table 7 on page 12*, *Table 8* and *Table 9 on page 13*) and programmable delay time. To minimize the component count the DELAY pin capacitor can be also omitted so the pin works as a normal Power Good.

5.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (0.85 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

Table 10. Uncompensated error amplifier characteristics

Description	Values
Transconductance	155 µS
Low frequency gain	100 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control. The error amplifier also determines the burst operation at light-load when the LCM is active.

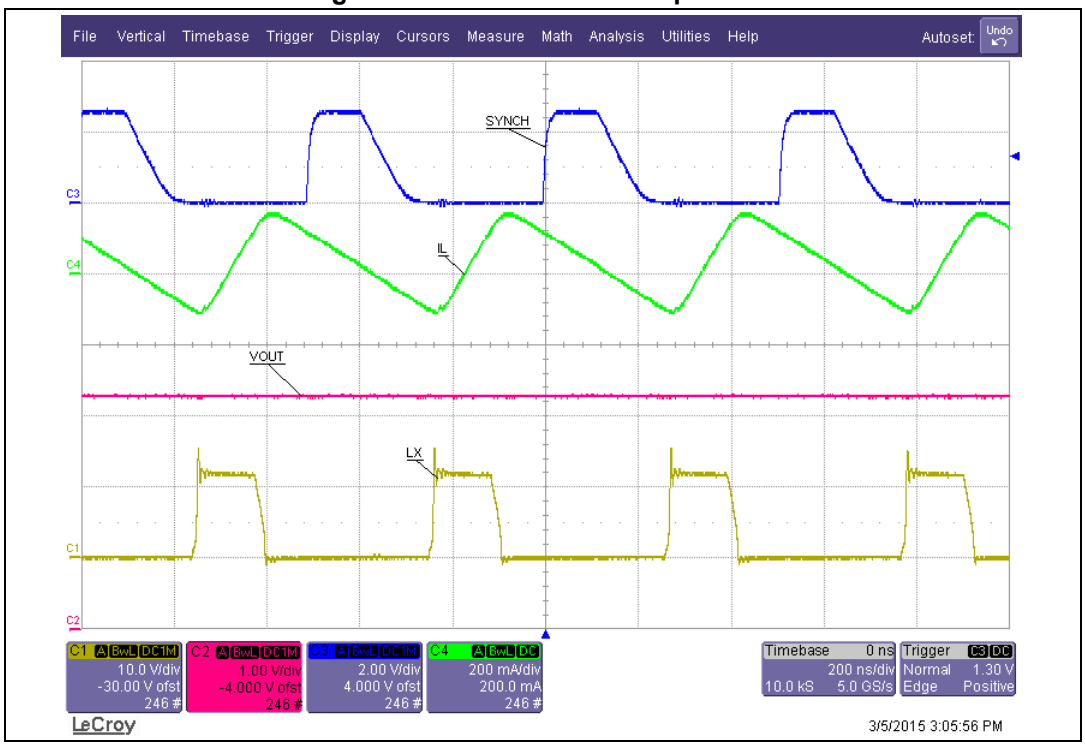
5.5 Light-load operation

The MLF pinstrapping during the power-up phase determines the light-load operation (refer to *Table 7 on page 12*, *Table 8* and *Table 9 on page 13*).

5.5.1 Low noise mode (LNM)

The low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}. The regulator in steady loading condition never skip pulses and it operates in continuous conduction mode (CCM) over the different loading conditions.

Figure 13. Low noise mode operation



Typical applications for the LNM operation are car audio, sensors.

5.5.2 Low consumption mode (LCM)

The low consumption mode maximizes the efficiency at light-load. The regulator prevents the switching activity whenever the switch peak current request is lower than the I_{SKIP} threshold (350 mA typical). As a consequence the A6985F device works in bursts and it minimizes the quiescent current request in the meantime between the switching operation.

In LCM operation, the pin SYNCH/ISKIP level dynamically defines the I_{SKIP} current threshold (see *Table 11*).

Table 11. I_{SKIP} current level

SYNCH / ISKIP (pin 4)	I_{SKIP} current threshold
LOW	$ISKIP_H$ = 0.35 A typical
HIGH	$ISKIP_L$ = 0.1 A typical

The ISKIP programmability helps to optimize the performance in terms of the output voltage ripple or efficiency at the light-load, that are parameters which disagree each other by definition.

A lower skip current level minimizes the voltage ripple but increases the switching activity (time between bursts gets closer) since less energy per burst is transfered to the output voltage at the given load. On the other side, a higher skip level reduces the switching activity and improves the efficiency at the light-load but worsen the voltage ripple.

No difference in terms of the voltage ripple and conversion efficiency for the medium and high load current level, that is when the device operates in the discontinuous or continuous mode (DCM vs. CCM).

Figure 14 and *Figure 15* report the efficiency measurements to highlight the $ISKIP_H$ and $ISKIP_L$ efficiency gap at the light-load also in comparison with the LNM operation. The same efficiency at the medium / high load is confirmed at different ISKIP levels.

Figure 14. Light-load efficiency comparison at different I_{SKIP} - linear scale

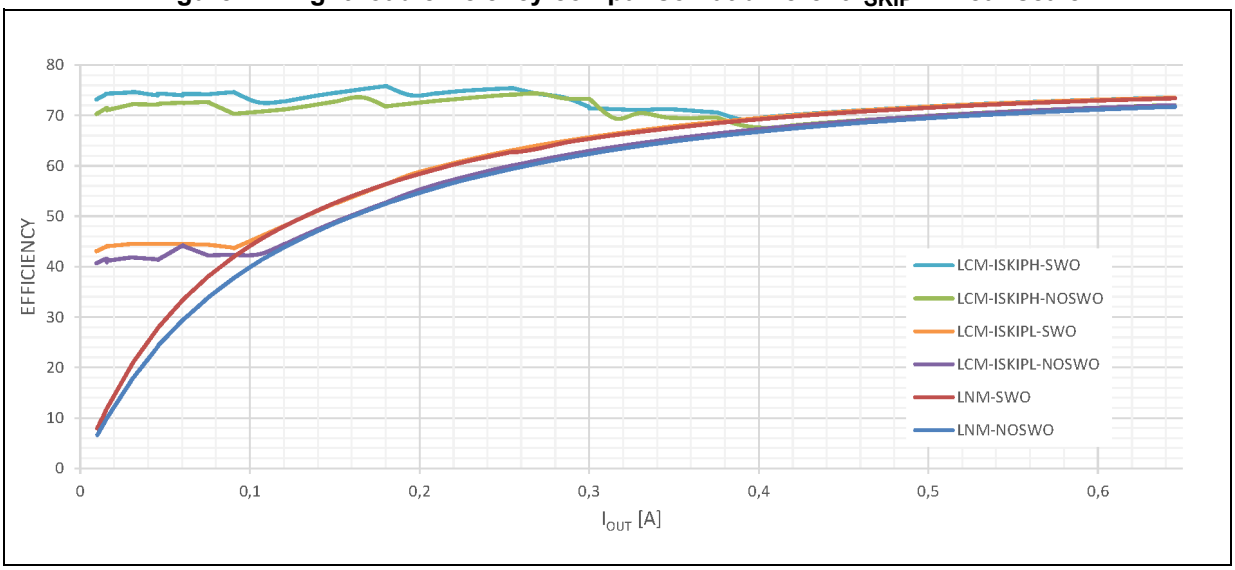


Figure 15. Light-load efficiency comparison at different I_{SKIP} - log scale

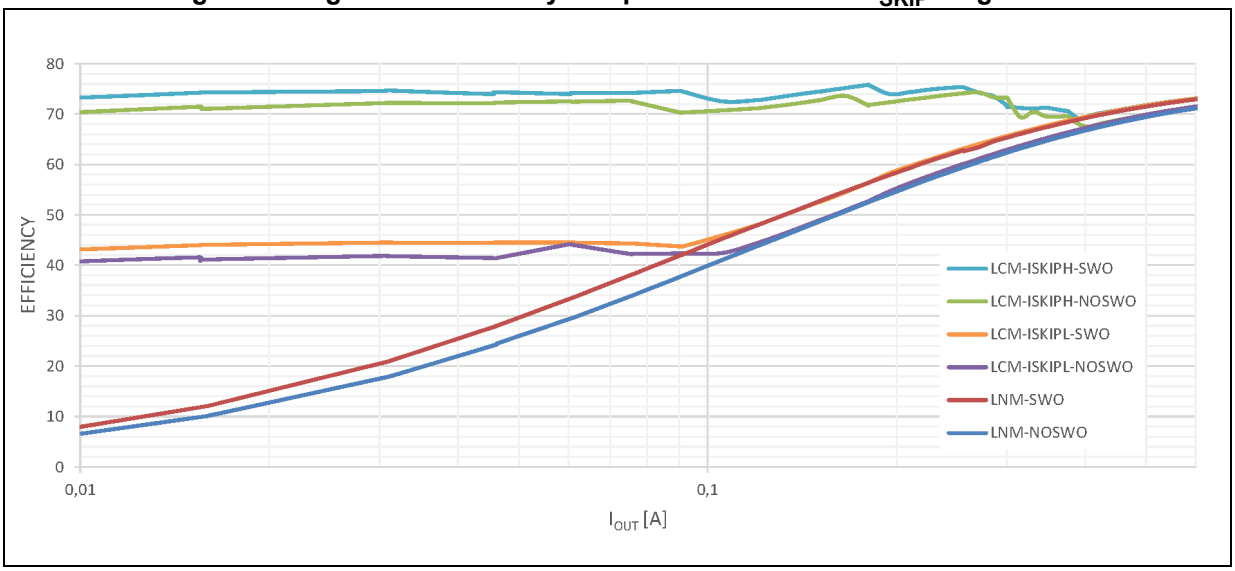


Figure 16 and *Figure 17* show the LCM operation at the different ISKIP level.

Figure 16 shows the $ISKIP_H$ = 350 mA typ. and so 34 mV output voltage ripple.

Figure 17 shows the $ISKIP_L$ = 100 mA typ. and so 13 mV output voltage ripple.

Figure 16. LCM operation with $ISKIP_H$ = 350 mA typ. at zero load

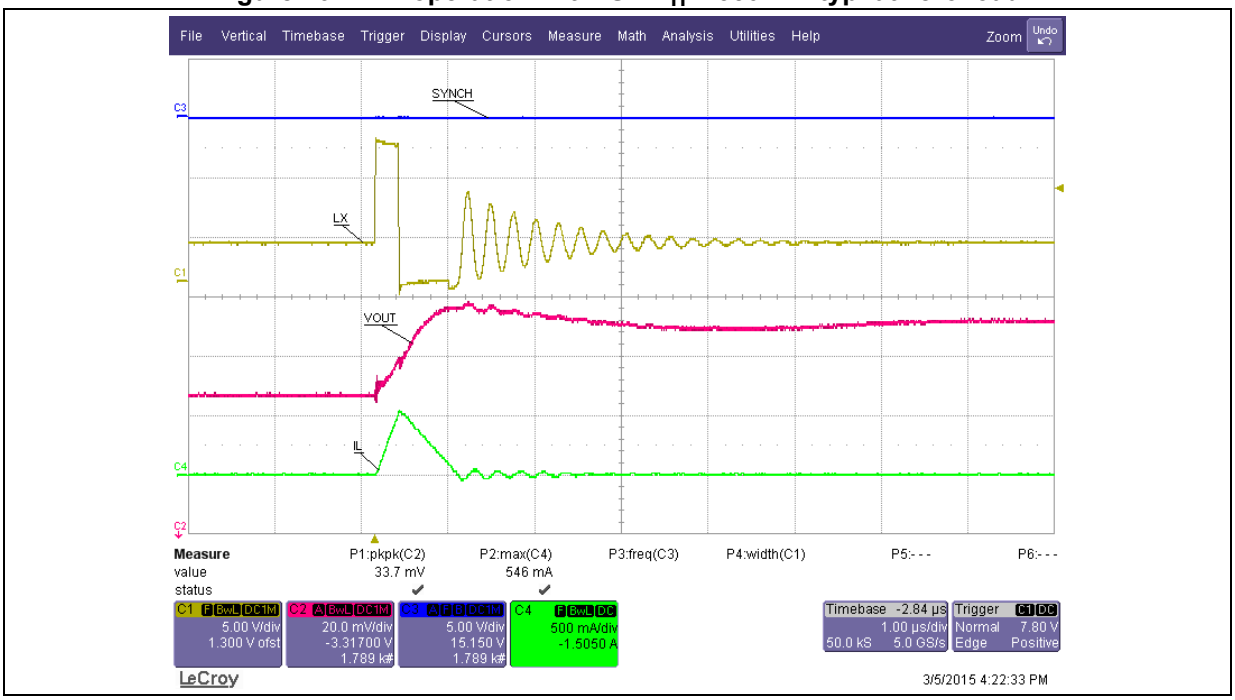
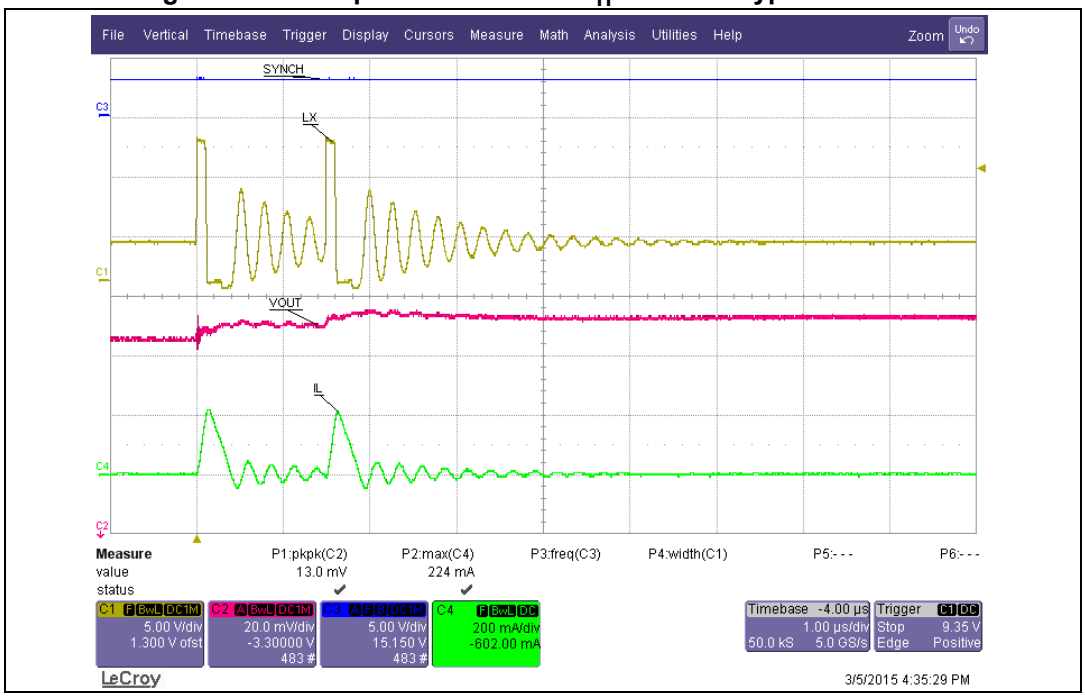


Figure 17. LCM operation with $ISKIP_H$ = 100 mA typ. at zero load



The LCM operation satisfies the requirements of the unswitched car body applications (KL30). These applications are directly connected to the battery and are operating when the engine is disabled. The typical load when the car is parked is represented by a CAN transceiver and a microcontroller in sleep mode (total load is around 20 - 30 µA). As soon as the transceiver recognizes a valid word in the bus, it awakes the µC and the rest of the application.

The typical input current request of the module when the car is parked is 100 µA typ. to prevent the battery discharge over the parking time. In order to minimize the regulator quiescent current request from the input voltage, the V_{BIAS} pin can be connected to an external voltage source in the range 3 V < V_{BIAS} < 5.5 V (see *Section 5.1: Power supply and voltage reference on page 16*).

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

Equation 13

$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (i_L(t) \cdot dt)}{C_{OUT}}$$

Figure 18. LCM operation over loading condition (part 1)

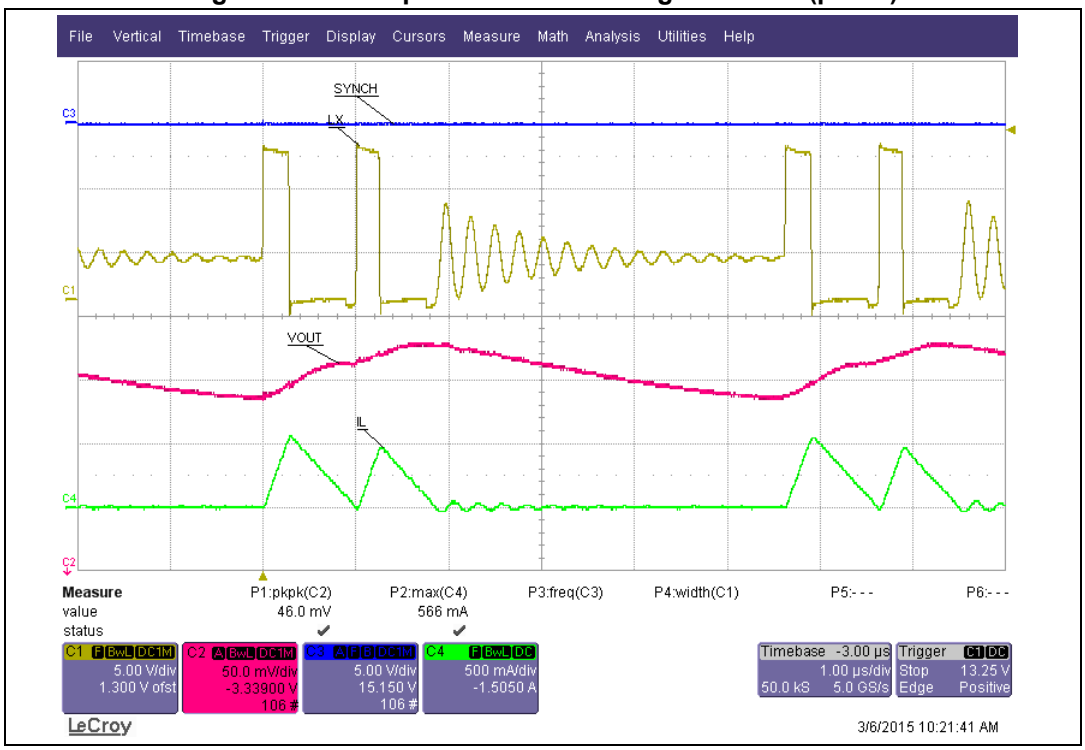


Figure 19. LCM operation over loading condition (part 2)

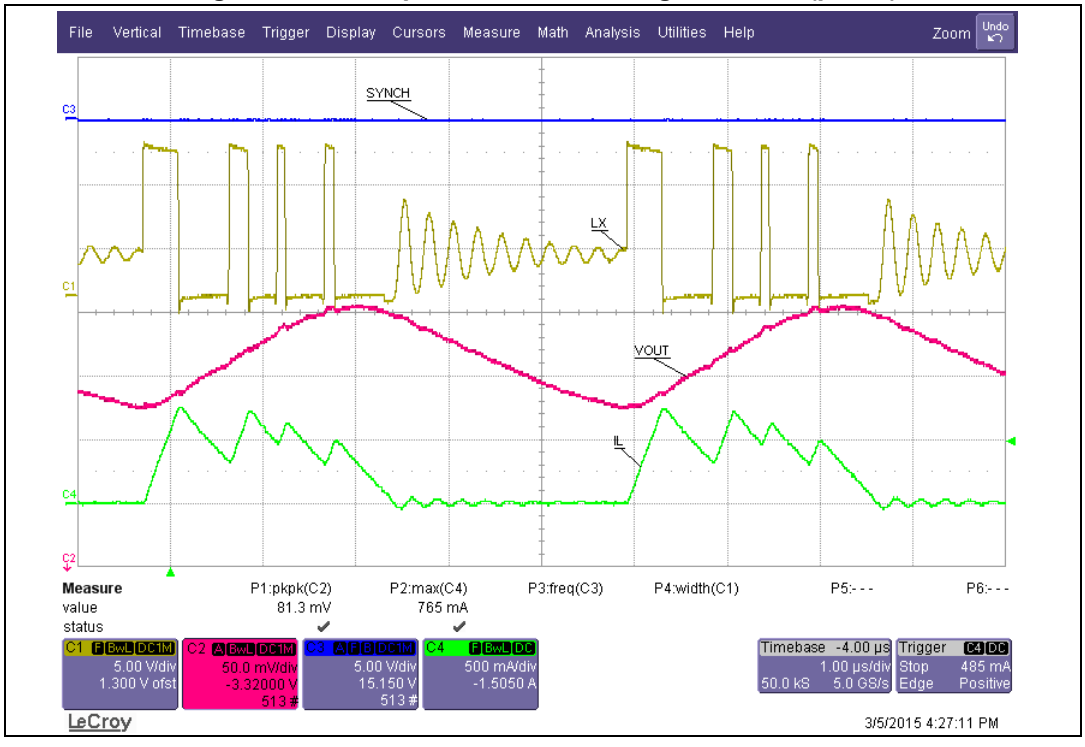
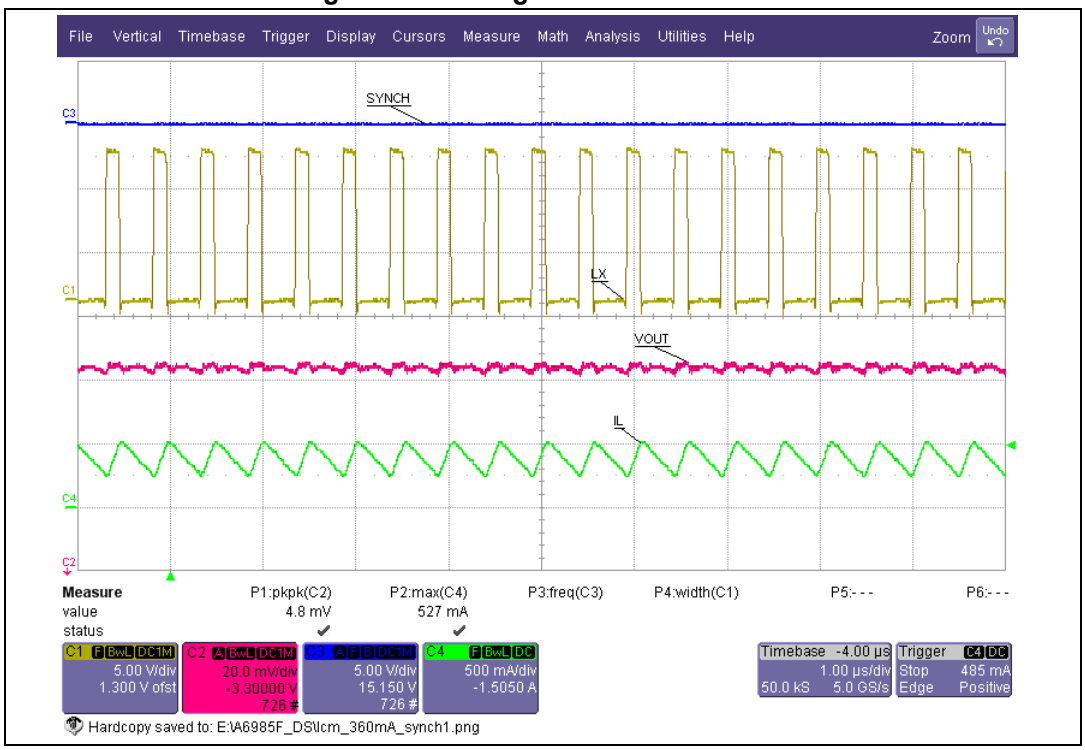


Figure 20. The regulator works in CCM



5.6 Switchover feature

The switchover maximizes the efficiency at light-load that is crucial for LCM applications.

5.6.1 LCM

The LCM operation satisfies the high efficiency requirements of the battery powered applications. In order to minimize the regulator quiescent current request from the input voltage, the V_{BIAS} pin can be connected to an external voltage source in the range $3\ V < V_{BIAS} < 5.5\ V$ (see *Section 5.1: Power supply and voltage reference on page 16*).

In case the V_{BIAS} pin is connected to the regulated output voltage (V_{OUT}), the total current drawn from the input voltage can be calculated as:

Equation 14

$$I_{QVIN} = I_{QOPVIN} + \frac{1}{\eta_{A6985F}} \bullet \frac{V_{BIAS}}{V_{IN}} \bullet I_{QOPVBIAS}$$

where $I_{Q\ OP\ VIN}$, $I_{Q\ OP\ VBIAS}$ are defined in *Table 5: Electrical characteristics on page 9* and η_{A6985F} is the efficiency of the conversion in the working point.

5.6.2 LNM

Equation 14 is also valid when the device works in LNM and it can increase the efficiency at medium load since the regulator always operates in continuous conduction mode.

5.7 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (see *Table 5: Electrical characteristics on page 9*) in overcurrent condition.

The A6985F device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. As a consequence, the peak current protection is disabled for a masking time after the high-side switch is turned on, the valley for a masking time after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The A6985F device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assure the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

The valley current threshold is designed higher than the peak to guarantee a proper operation. In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn on, so the device can skip pulses decreasing the swathing frequency.

Figure 21. Valley current sense operation in overcurrent condition

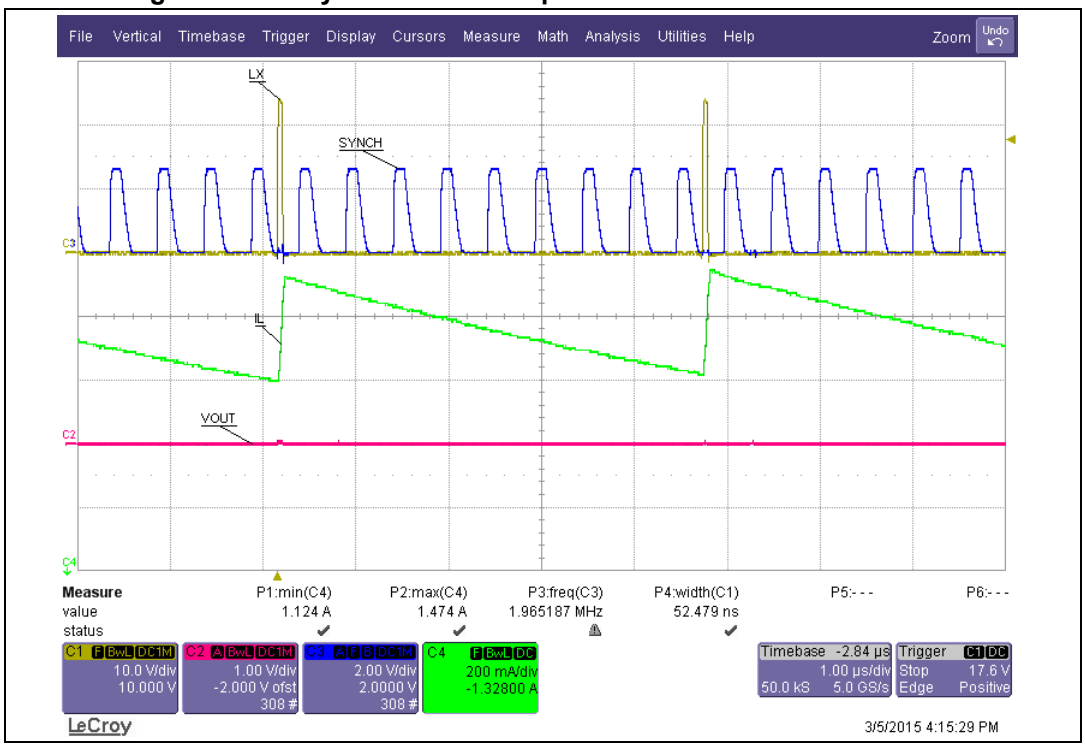


Figure 21 shows the switching frequency reduction during the valley current sense operation in case of extremely low duty cycle (V_{IN} =38 V, f_{SW} = 2 MHz short-circuit condition).

In a worst case scenario (like *Figure 21*) of the overcurrent protection the switch current is limited to:

Equation 15

$$I_{MAX} = I_{VALLEYTH} + \frac{V_{IN} - V_{OUT}}{L} \bullet T_{MASKHS}$$

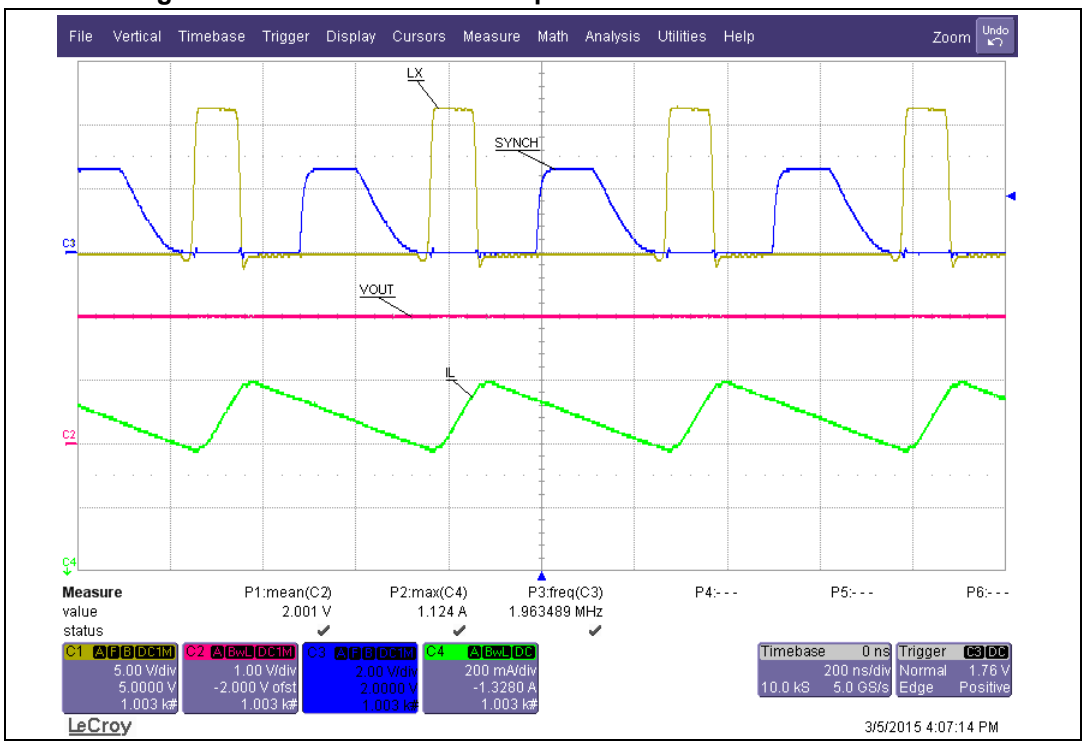
where I_{VALLEY_TH} is the current threshold of the valley sensing circuitry (see *Table 5: Electrical characteristics on page 9*) and T_{MASK_HS} is the masking time of the high-side switch 100 nsec. typ.).

In most of the overcurrent conditions the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

Equation 16

$$I_{MAX} = I_{PEAK\_TH}$$

Figure 22. Peak current sense operation in overcurrent condition



The DC current flowing in the load in overcurrent condition is:

Equation 17

$$I_{DCOC}(V_{OUT}) = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - \left(\frac{V_{IN} - V_{OUT}}{2 \bullet L} \bullet T_{ON}\right)$$

OCP and switchover feature

Output capacitor discharging the current flowing to ground during heavy short-circuit events is only limited by parasitic elements like the output capacitor ESR and short-circuit impedance.

Due to parasitic inductance of the short-circuit impedance, negative output voltage oscillations can be generated with huge discharging current levels (see *Figure 23*).

Figure 23. Output voltage oscillations during heavy short-circuit

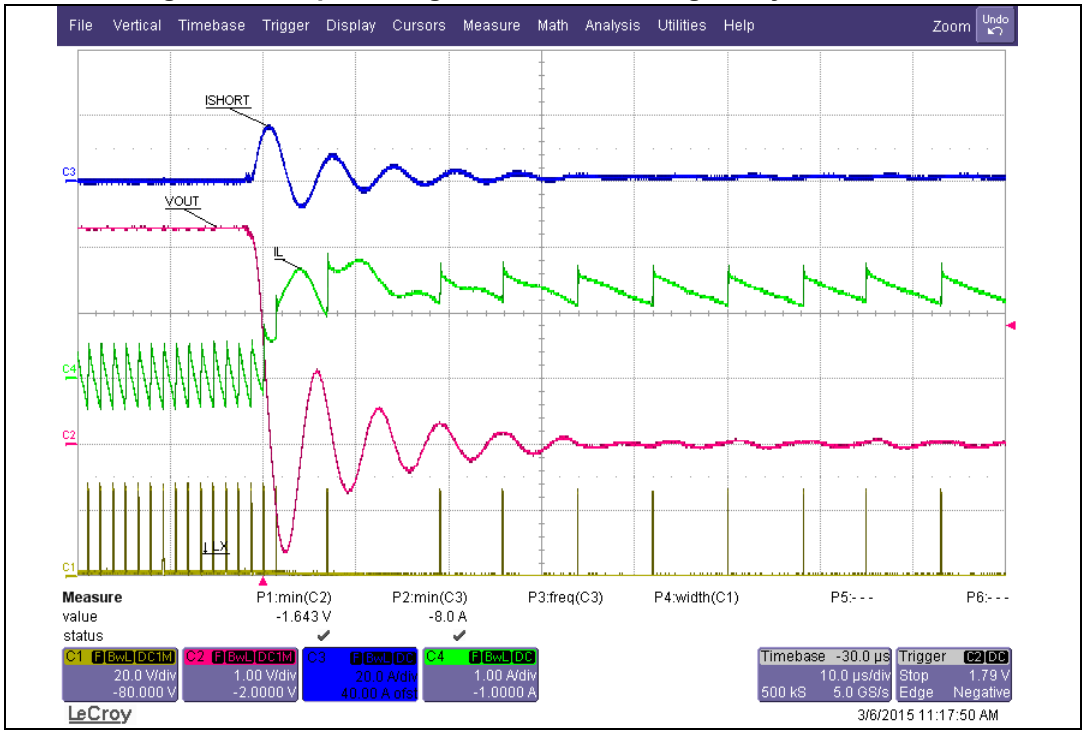
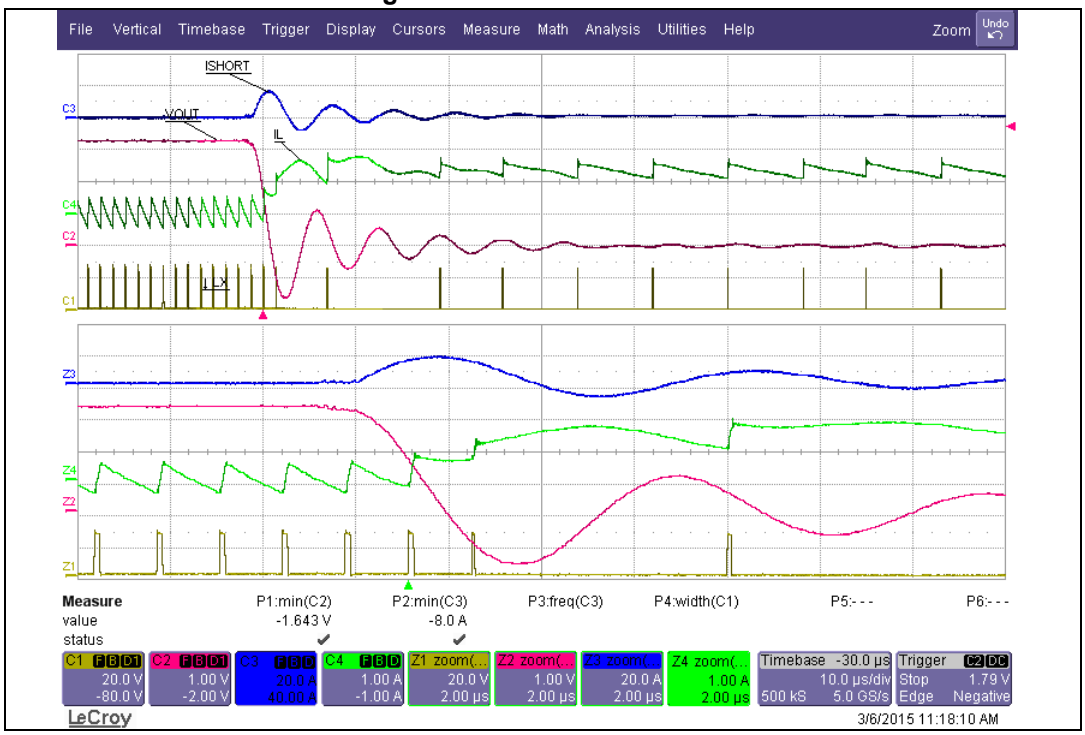


Figure 24. Zoomed waveform

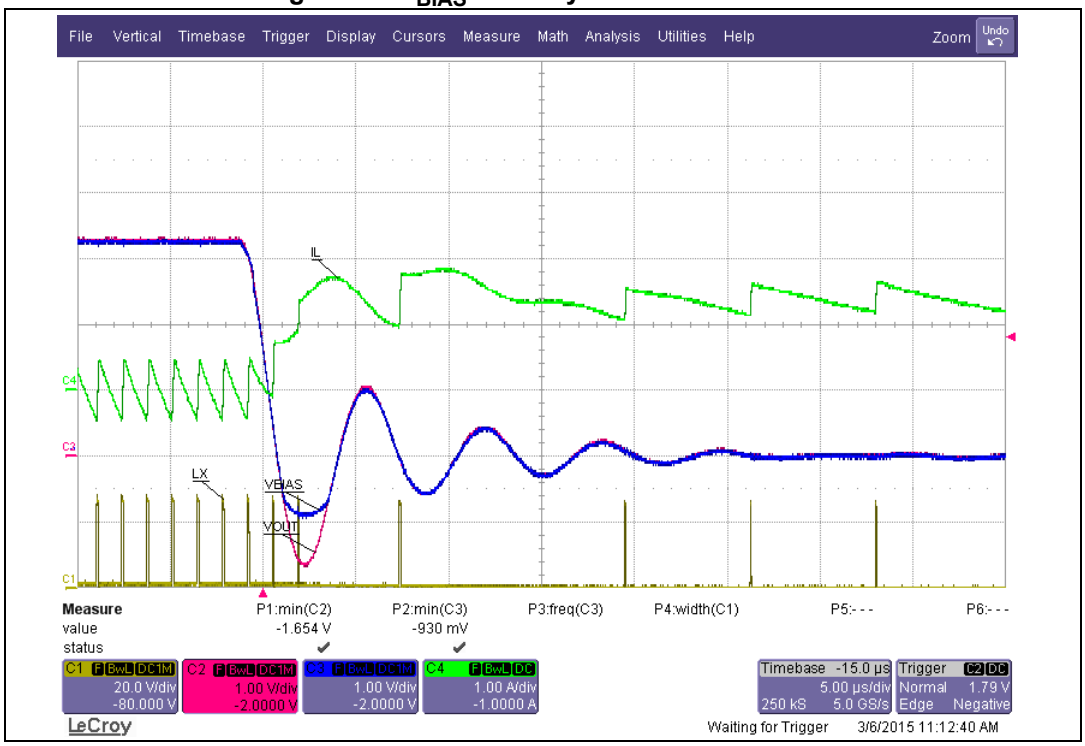


The V_{BIAS} pin absolute maximum ratings (see *Table 2: Absolute maximum ratings on page 7*) must be satisfied over the different dynamic conditions.

If V_{BIAS} is connected to GND there are no issues (see *Figure 23* and *Figure 24*).

A small resistor value (few Ω) in series with the V_{BIAS} can help to limit the pin negative voltage (see *Figure 25*) during heavy short-circuit events if it is connected to the regulated output voltage.

Figure 25. V_{BIAS} in heavy short-circuit event



5.8 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value.

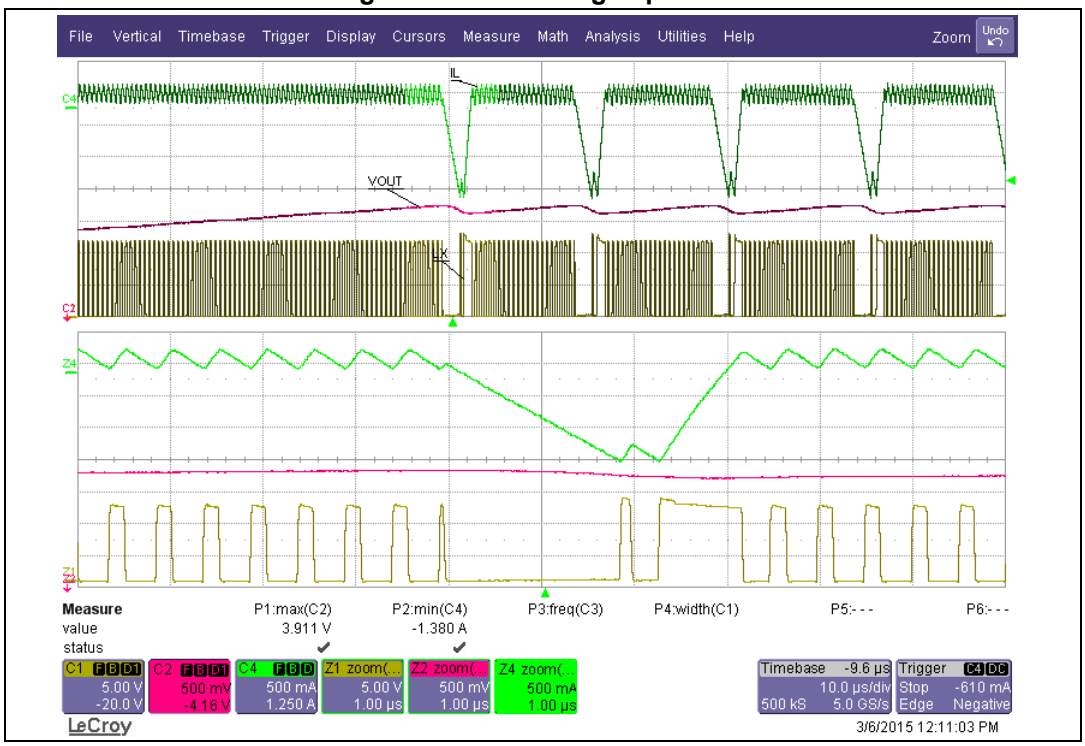
This is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst case scenario in term of load transitions.

The protection is reliable and also able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. As a consequence the output voltage regulation would be affected.

Figure 26 shows the overvoltage operation during a negative steep load transient for a system designed with huge inductor value and small output capacitor. The inductor value limits the switch current slew rate and the extra charge flowing into the small capacitor value generates an overvoltage event. This can be considered as an example for a system with dynamic performance not in line with the load request.

The A6985F device implements a 1 A typ. negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

Figure 26. Overvoltage operation

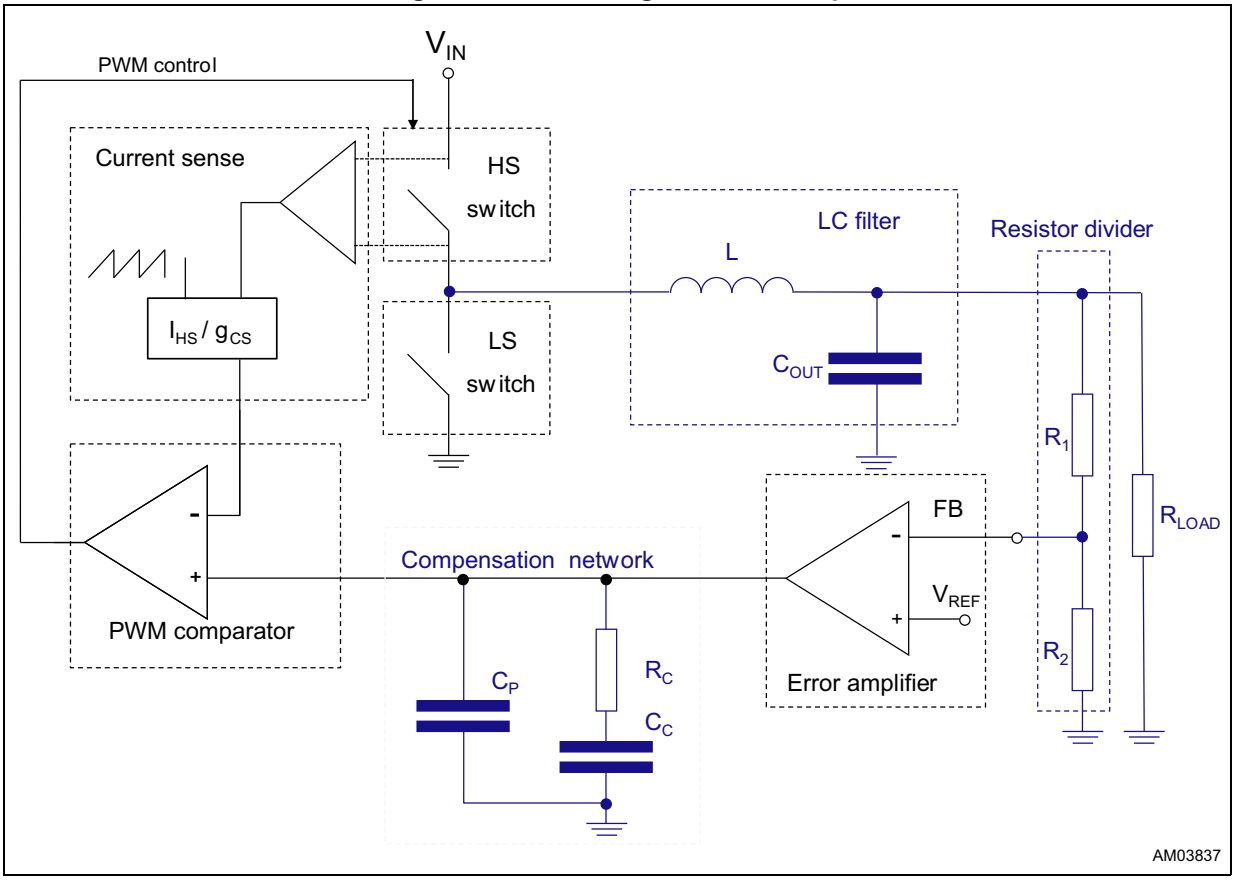


5.9 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (165 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

6 Closing the loop

Figure 27. Block diagram of the loop



6.1 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

Equation 18

$$G_{CO(s)} = R_{LOAD} \bullet g_{cs} \bullet \frac{1}{1 + \frac{R_{LOAD} \bullet T_{SW}}{L} \bullet [m_C \bullet (1 - D) - 0.5]} \bullet \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \bullet F_H(s)$$

where R_{LOAD} represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry, ω_p the single pole introduced by the power stage and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 19

$$\omega_z = \frac{1}{ESR \bullet C_{OUT}}$$

Equation 20

$$\omega_p = \frac{1}{R_{LOAD} \bullet C_{OUT}} + \frac{m_c \bullet (1 - D) - 0.5}{L \bullet C_{OUT} \bullet f_{SW}}$$

where:

Equation 21

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{PP} \cdot g_{CS} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases}$$

S_n represents the on time slope of the sensed inductor current, S_e the on time slope of the external ramp (V_{PP} peak-to-peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

S_e can be calculated from the parameter $V_{PP} \times g_{CS}$ given in *Table 5 on page 9*.

The sampling effect contribution $F_H(s)$ is:

Equation 22

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \bullet Q_p} + \frac{s^2}{\omega_n^2}}$$

where:

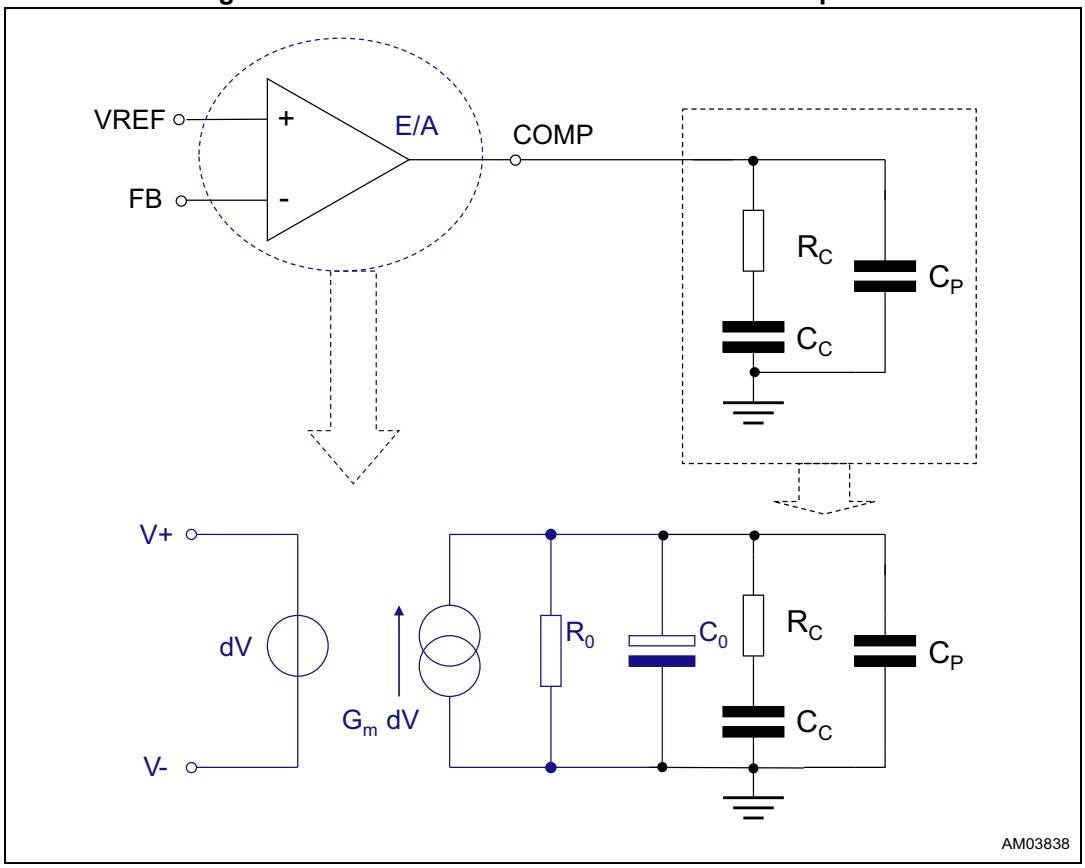
Equation 23

$$Q_p = \frac{1}{\pi \bullet [m_c \bullet (1 - D) - 0.5]}$$

6.2 Error amplifier compensation network

The typical compensation network required to stabilize the system is shown in *Figure 28*.

Figure 28. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

Equation 24

$$A_0(s) = \frac{A_{V0} \bullet (1 + s \bullet R_c \bullet C_c)}{s^2 \bullet R_0 \bullet (C_0 + C_p) \bullet R_c \bullet C_c + s \bullet (R_0 \bullet C_c + R_0 \bullet (C_0 + C_p) + R_c \bullet C_c) + 1}$$

Where $A_{vo} = G_m \cdot R_o$

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 25

$$f_{PLF} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet C_c}$$

Equation 26

whereas the zero is defined as:

$$f_{PHF} = \frac{1}{2 \bullet \pi \bullet R_0 \bullet (C_0 + C_p)}$$

Equation 27

$$f_Z = \frac{1}{2 \bullet \pi \bullet R_c \bullet C_c}$$

6.3 Voltage divider

6.3.1 Internal voltage divider

In the A6985F3V3 and A6985F5V, the voltage divider contribution is equal to:

Equation 28

$$G_{DIV}(s) = G_{DIV,INT}(s) = \frac{V_{REF}}{V_{OUT}} = \begin{cases} \frac{0.85}{3.3} = 0.2576 & \textbf{A6985F3V3} \\ \frac{0.85}{5} = 0.17 & \textbf{A6985F5V} \end{cases}$$

6.3.2 External voltage divider

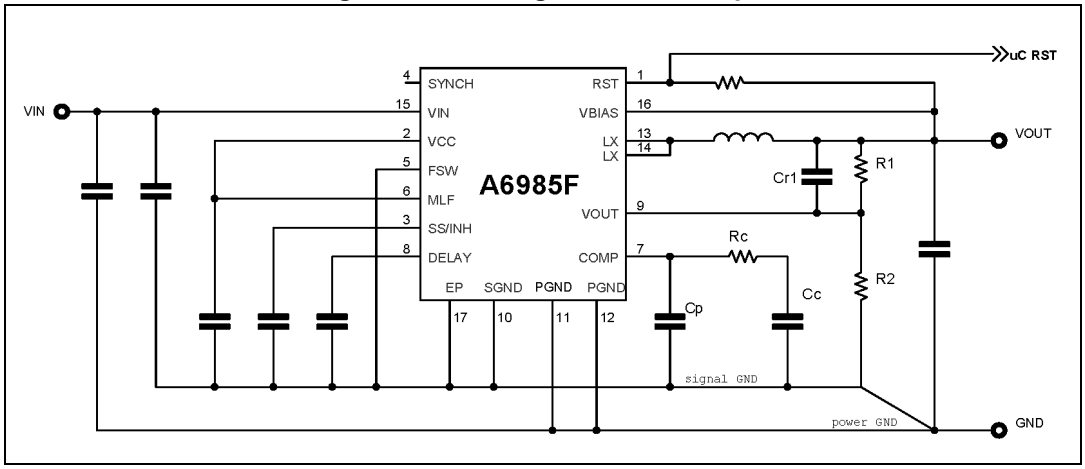
In the A6985F the simple voltage divider contribution is:

Equation 29

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \bullet G_{DIV,INT}(s) = \frac{R_2}{R_1 + R_2} \quad \textbf{A6985F}$$

A small signal capacitor in parallel to the upper resistor (see *Figure 29*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin.

Figure 29. Leading network example



Laplace transformer of the leading network:

Equation 30

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \bullet \frac{(1 + s \bullet R_1 \bullet C_{R1})}{\left(1 + s \bullet \frac{R_1 \bullet R_2}{R_1 + R_2} \bullet C_{R1}\right)}$$

where:

Equation 31

$$f_Z = \frac{1}{2 \bullet \pi \bullet R_1 \bullet C_{R1}}$$

$$f_p = \frac{1}{2 \bullet \pi \bullet \frac{R_1 \bullet R_2}{R_1 + R_2} \bullet C_{R1}}$$

$$f_Z < f_p$$

6.4 Total loop gain

In summary, the open loop gain can be expressed as:

Equation 32

$$G(s) = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_0(s)$$

Example 1

A6985F3V3 with V_{IN} = 12 V and R_{OUT} = 6.6Ω

Selecting L = 4.7µH, C_{OUT} = 10 µF and ESR = 1 mΩ, R_C= 110 kΩ, C_C= 68 pF, C_P = 1.2 pF (please refer to *Example 2*), the gain and phase bode diagrams are plotted respectively in *Figure 30* and *Figure 31*.

Equation 33

$$BW = 112kHz$$

$$\text{phase margin} = 67^0$$

Figure 30. Module plot

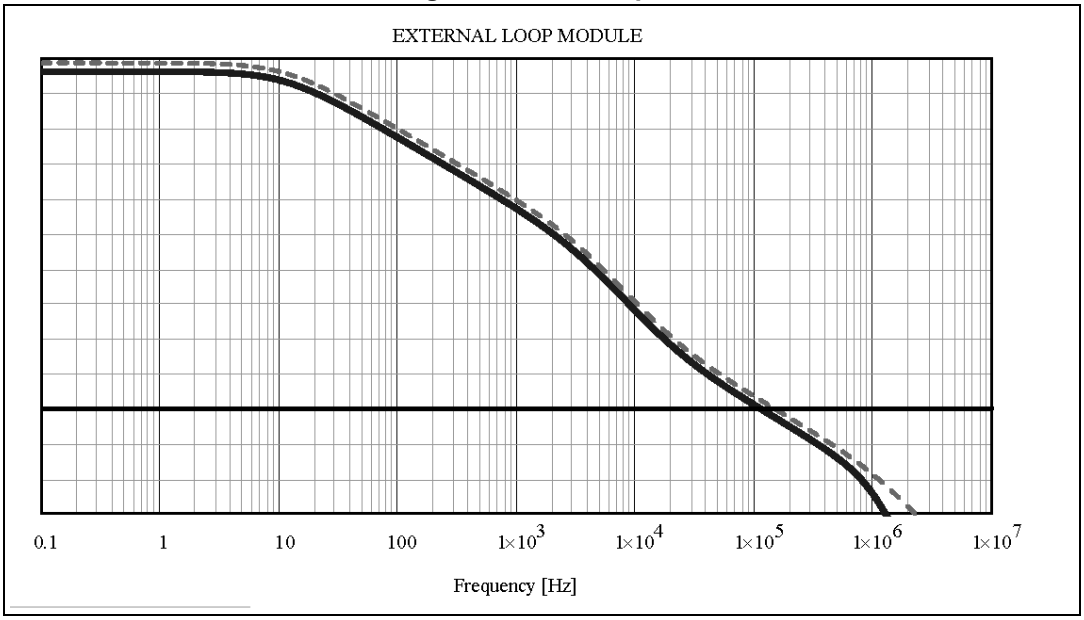
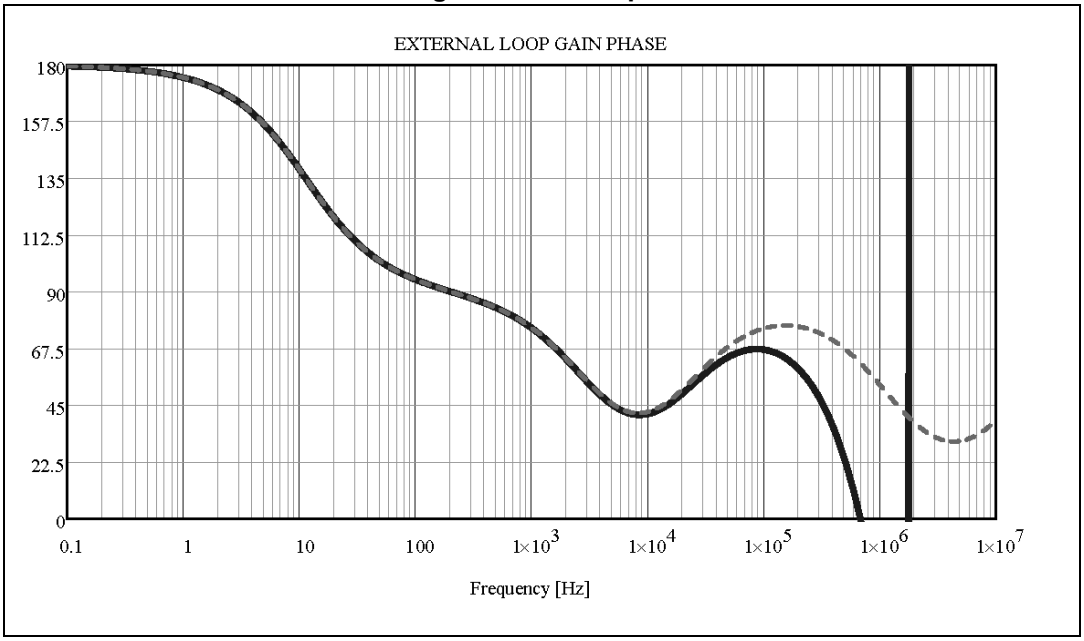


Figure 31. Phase plot



The solid trace represents the transfer function including the sampling effect term (see *Equation 22 on page 40*), the dotted trace neglects the contribution.

6.5 Compensation network design

The maximum bandwidth of the system can be designed up to $f_{SW}/6$ or up to 150 kHz to guarantee a valid small signal model.

Equation 34

$$BW = \min\left(\frac{f_{SW}}{6}, 150kHz\right)$$

Equation 35

$$R_C = \frac{2 \cdot \pi \cdot BW \cdot C_{OUT} \cdot V_{OUT}}{0.85V \cdot g_{CS} \cdot g_{m\,TYP}}$$

where g_{CS} represents the current sense transconductance (see *Table 5: Electrical characteristics on page 9*) and $g_{m\,TYP}$ the error amplifier transconductance.

Equation 36

$$C_C = \frac{5}{2 \cdot \pi \cdot R_C \cdot BW}$$

Example 2

Considering A6985F3V3, V_{IN} = 12 V, L = 4.7 µH, C_{OUT} = 10 µF, f_{SW} = 2 MHz.

Assuming to design the compensation network to achieve a system bandwidth of 110 kHz:

Equation 37

$$f_{POLE} = 2.4kHz$$

Equation 38

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} = 6.6\Omega$$

so accordingly with *Equation 35* and *Equation 36*:

Equation 39

$$R_C = 107k\Omega \approx 110k\Omega$$

Equation 40

$$C_C = 66pF \approx 68pF$$

7 Application notes

7.1 Output voltage adjustment

In A6985F3V3 and A6985F5V the output voltage is fixed by an internal divider $G_{DIV\ INT}$ (see *Table 5 on page 9*).

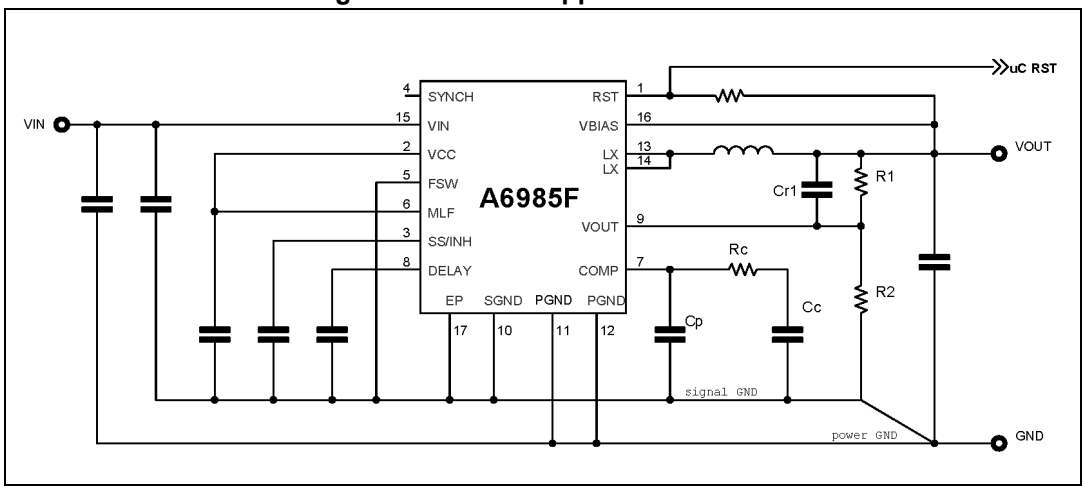
In A6985F the internal reference is equal to 0.85 V typical, and the output voltage is adjusted accordingly to *Equation 41* (see *Figure 32*):

Equation 41

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R_1}{R_2}\right) = 0.85 \bullet \left(1 + \frac{R_1}{R_2}\right)$$

where C_{r1} capacitor is sometimes useful to increase the small signal phase margin (please refer to *Section 6.5: Compensation network design*).

Figure 32. A6985F application circuit



7.2 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN.

Please refer to *Table 6: f_{SW} selection on page 12* to identify the pull-up / pull-down resistor value. f_{SW} = 250 kHz / f_{SW} = 500 kHz preferred codifications don't require any external resistor.

7.3 MLF pin

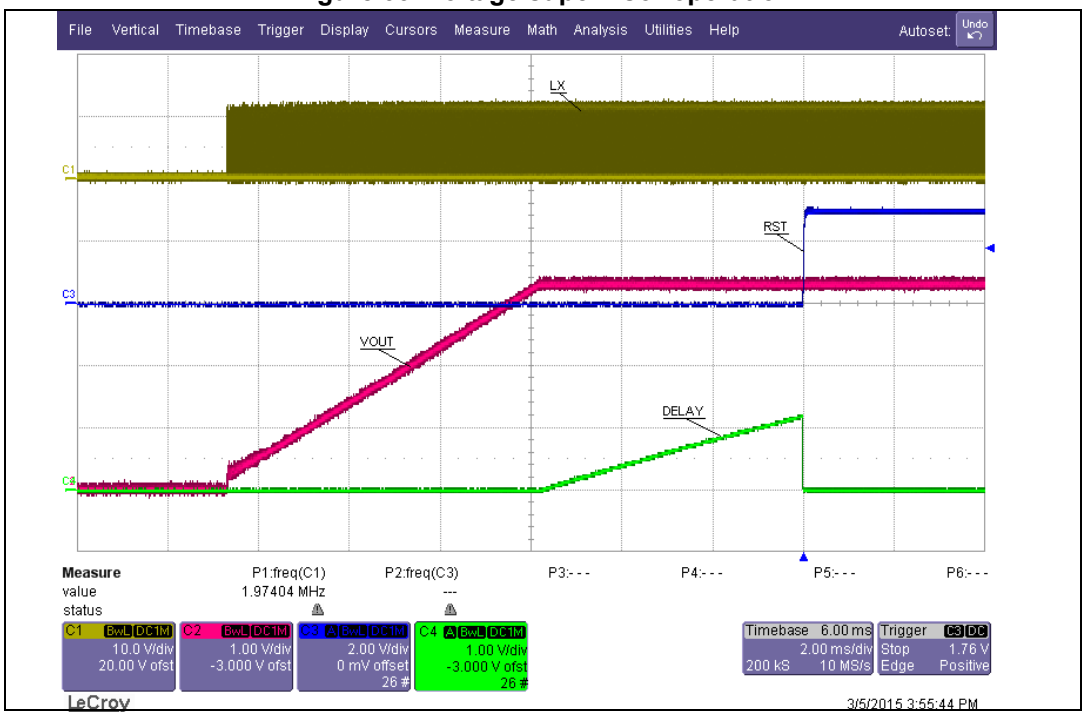
A resistor connected to the MLF pin features the selection of the between low noise mode / low consumption mode and the different RST thresholds. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN.

Please refer to *Table 7 on page 12*, *Table 8*, and *Table 9 on page 13* to identify the pull-up / pull-down resistor value. (LNM, RST threshold 93%) / (LCM, RST threshold 93%) preferred codifications don't require any external resistor.

7.4 Voltage supervisor

The embedded voltage supervisor (composed of the RST and the DELAY pins) monitors the regulated output voltage and keeps the RST open collector output in low impedance as long as the V_{OUT} is out of regulation. In order to ensure a proper reset of digital devices with a valid power supply, the device can delay the RST assertion with a programmable time.

Figure 33. Voltage supervisor operation



The comparator monitoring the FB voltage has four different programmable thresholds (80%, 87%, 93%, 96% nominal output voltage) for high flexibility (see *Section 7.3: MLF pin*, *Table 7 on page 12*, *Table 8*, and *Table 9 on page 13*).

When the RST comparator detects the output voltage is in regulation, a 2 µA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V (see *Figure 33*).

The C_{DELAY} is dimensioned accordingly with *Equation 42*:

Equation 42

$$C_{DELAY} = \frac{I_{SSCH} \bullet T_{DELAY}}{V_{DELAY}} = \frac{2\mu A \bullet T_{DELAY}}{1.234V}$$

The maximum suggested capacitor value is 270 nF.

7.5 Synchronization (LNM)

Beating frequency noise is an issue when multiple switching regulators populate the same application board. The A6985F synchronization circuitry features the same switching frequency for a set of regulators simply connecting their SYNCH pin together, so preventing beating noise. The master device provides the synchronization signal to the others since the SYNCH pin is I/O able to deliver or recognize a frequency signal.

For proper synchronization of multiple regulators, all of them have to be configured with the same switching frequency (see *Table 6 on page 12*), so the same resistor connected at the FSW pin.

In order to minimize the RMS current flowing through the input filter, the A6985F device provides a phase shift of 180° between the master and the SLAVES. If more than two devices are synchronized, all slaves will have a common 180° phase shift with respect to the master.

Considering two synchronized A6985F which regulates the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is optimized and is calculated as:

Equation 43

$$I_{RMS} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1-2D)} & \text{if } D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D-1) \cdot (2-2D)} & \text{if } D > 0.5 \end{cases}$$

The graphical representation of the input RMS current of the input filter in the case of two devices with 0° phase shift (synchronized to an external signal) or 180° phase shift (synchronized connecting their SYNCH pins) regulating the same output voltage is provided in *Figure 34*. To dimension the proper input capacitor please refer to *Section 7.6.1: Input capacitor selection on page 53*.

Figure 34. Input RMS current

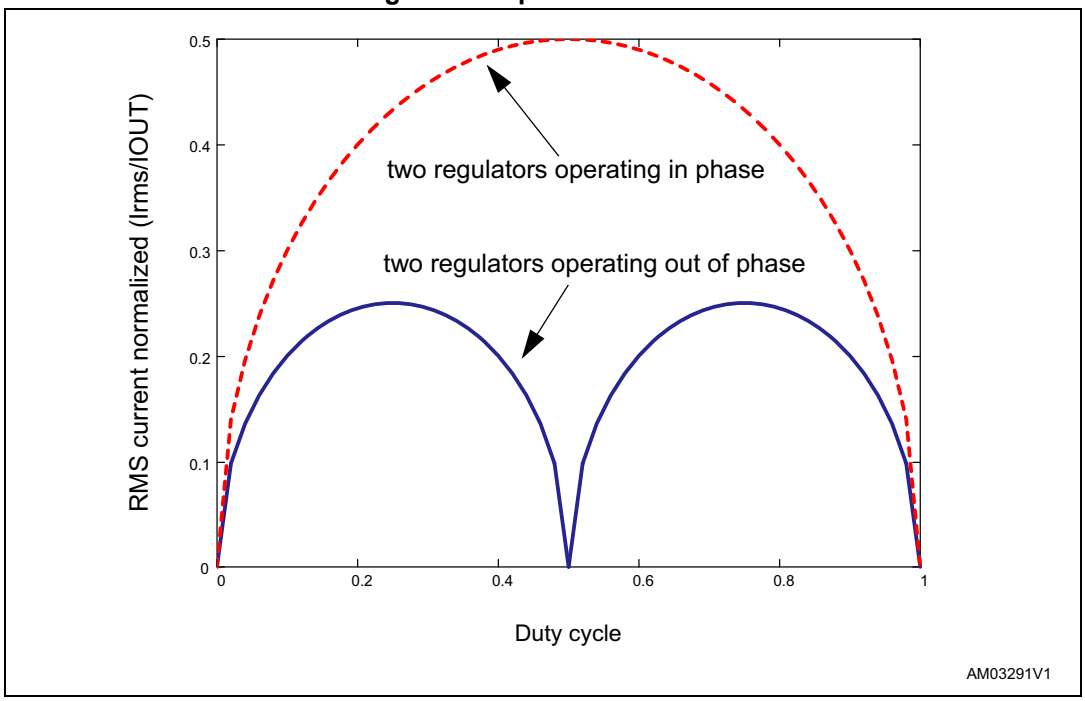


Figure 35 shows two regulators not synchronized.

Figure 35. Two regulators not synchronized

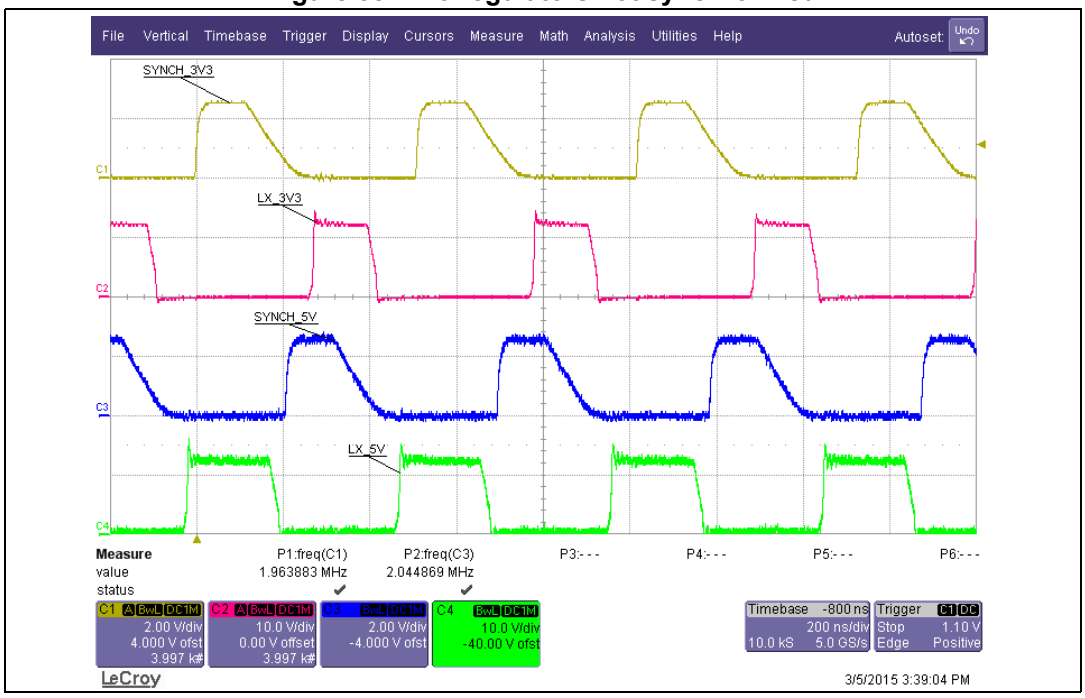
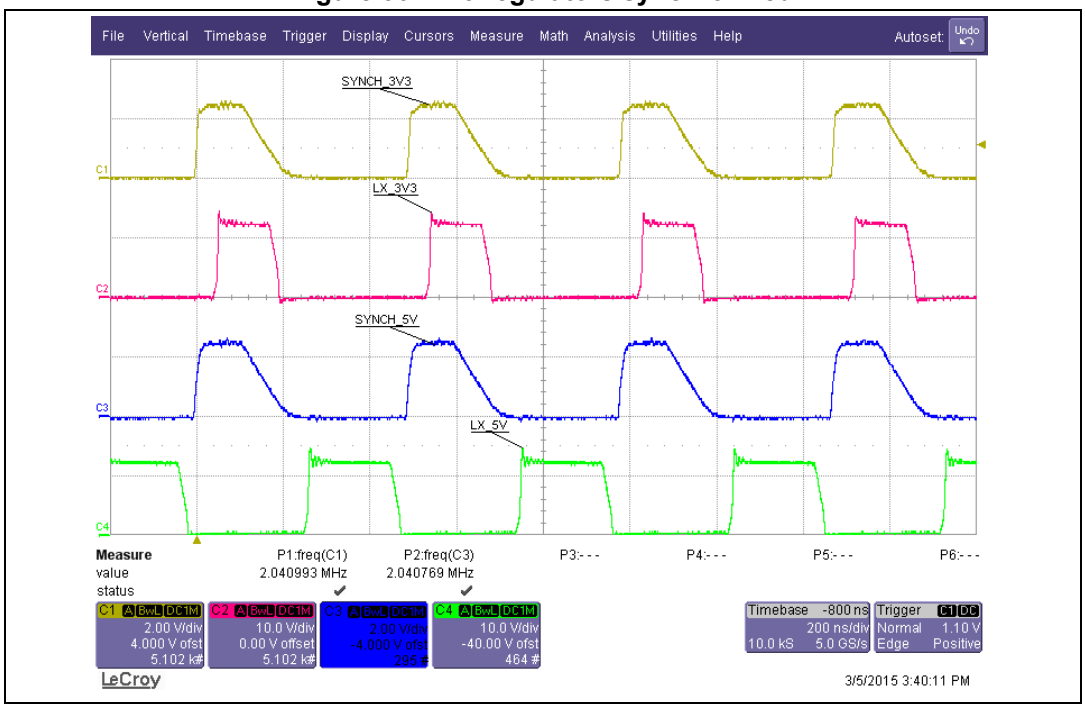


Figure 36 shows the same regulators working synchronized. The MASTER regulator (LX_5V trace) delivers the synchronization signal (SYNCH_3V3, SYNCH_5V pins are connected together) to the SLAVE device (LX_3V3). The SLAVE regulator works in phase with the synchronization signal which is out of phase with the MASTER switching operation.

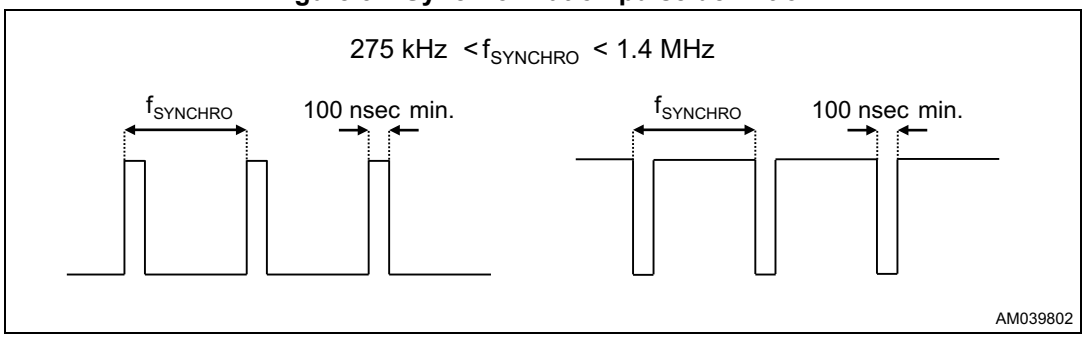
Figure 36. Two regulators synchronized



Multiple A6985F devices can be synchronized to an external frequency signal fed to the SYNCH pin. In this case the regulator set is phased to the reference and all the devices will work with 0° phase shift.

The frequency range of the synchronization signal is 275 kHz - 1.4 MHz and the minimum pulse width is 100 nsec (see *Figure 37*).

Figure 37. Synchronization pulse definition



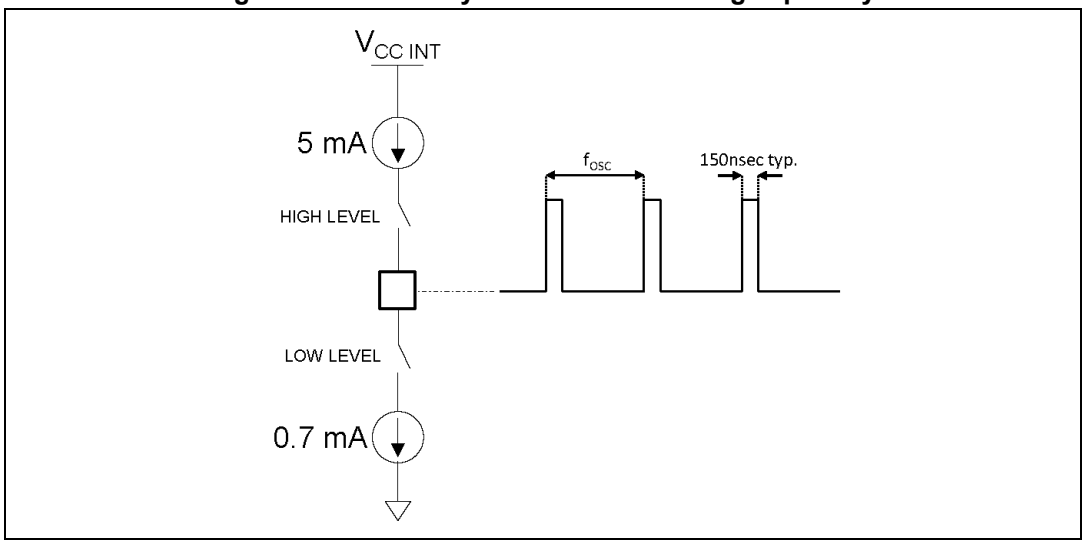
Since the slope compensation contribution that is required to prevent subharmonic oscillations in peak current mode architecture depends on the switching frequency, it is important to select the same oscillator frequency for all regulators (all of them operate as SLAVE) as close as possible to the frequency of the reference signal (please refer to *Table 6: f_{SW} selection on page 12*). As a consequence all the regulators have the same resistor value connected to the FSW pin, so the slope compensation is optimized

accordingly with the frequency of the synchronization signal. The slope compensation contribution is latched at power-up and so fixed during the device operation.

The A6985F normally operates in MASTER mode, driving the SYNCH line at the selected oscillator frequency as shown in *Figure 35* and *Figure 36*.

In SLAVE mode the A6985F sets the internal oscillator at 250 kHz typ. (see *Table 6 on page 12* - first row) and drives the line accordingly.

Figure 38. A6985F synchronization driving capability



In order to safely guarantee that each regulator recognizes itself in SLAVE mode during the normal operation, the external master must drive the SYNCH pin with a clock signal frequency higher than the maximum oscillator spread (refer to *Table 6*) for at least 10 internal clock cycles.

For example: selecting R_{FSW} = 0 W to GND

Table 12. Example of oscillator frequency selection from *Table 6*

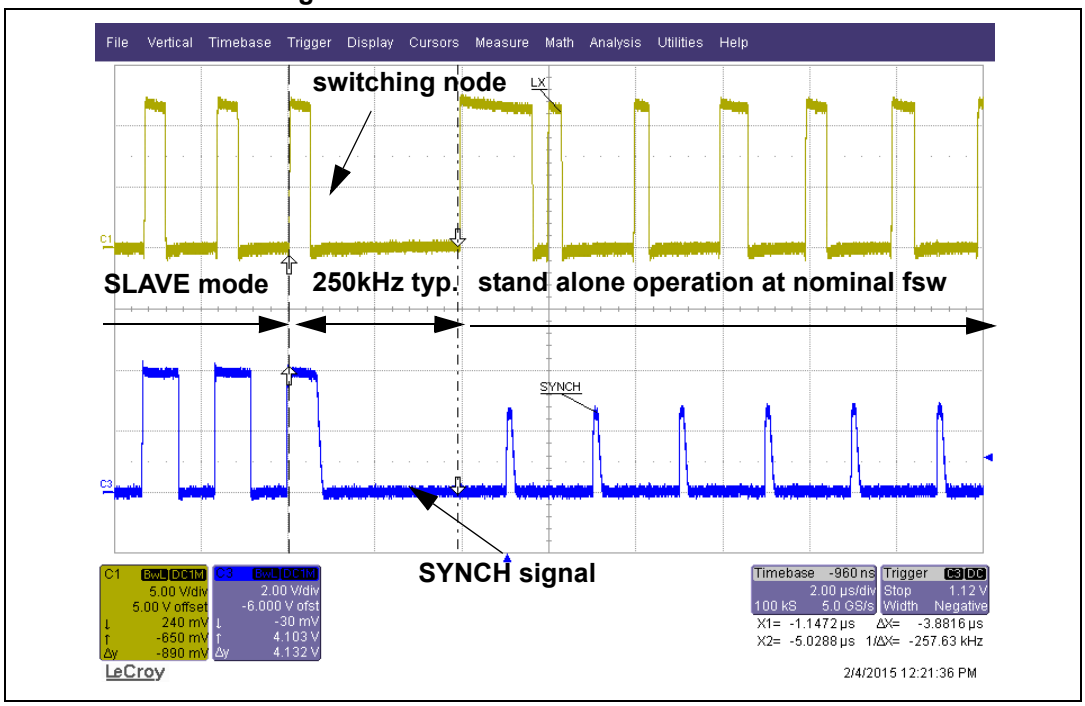
Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	f_{SW} min.	f_{SW} typ.	f_{SW} max.
f_{SW}	NC	0 Ω	450	500	550

the device enters in slave mode after 10 pulses at frequency higher than 550 kHz and so it is able to synchronize to a clock signal in the range 275 kHz - 1.4 MHz (see *Figure 37*).

Anyway it is suggested to limit the frequency range within ± 20% f_{SW} resistor nominal frequency (see details in text below). If not spread spectrum is required, all the regulators synchronize to a frequency higher to the maximum oscillator spread (550 kHz in the example).

The device keeps operating in slave mode as far as the master is able to drive the SYNCH pin faster than 275 kHz (maximum oscillator spread for 250 kHz oscillator), otherwise it goes back into MASTER mode at the nominal oscillator frequency after successfully driving one pulse at 250 kHz (see *Figure 39*) in the SYNCH line.

Figure 39. Slave to master mode transition

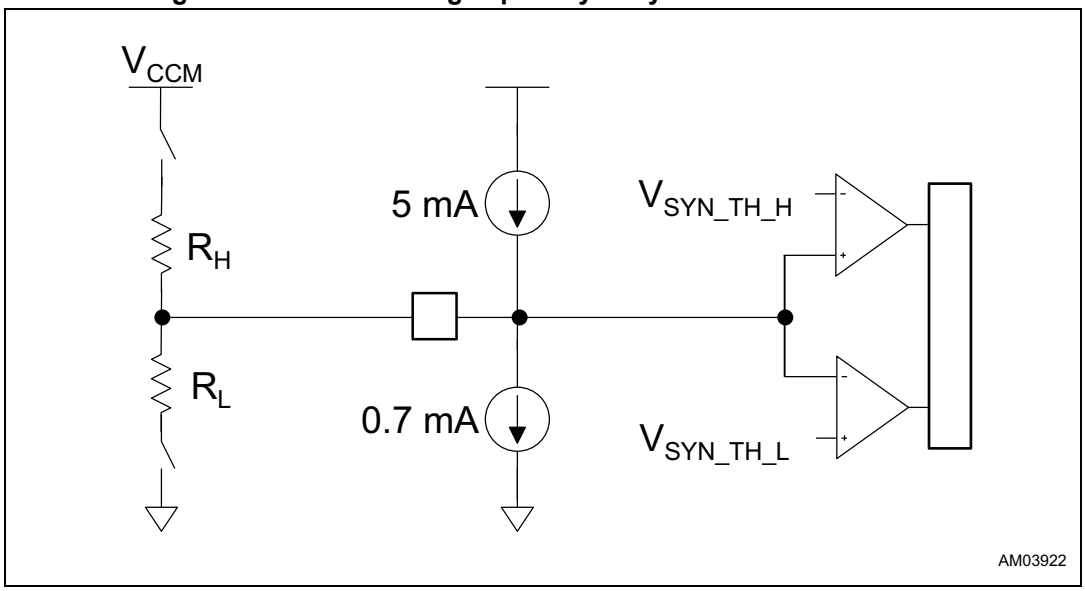


The external master can force a latched SLAVE mode driving the SYNCH pin low at power-up, before the soft-start starts the switching activity. So the oscillator frequency is 250 kHz typ. fixed until a new UVLO event is triggered regardless FSW resistor value, that otherwise counts to design the slope compensation. The same considerations above are also valid.

The master driving capability must be able to provide the proper signal levels at the SYNCH pin (see *Table 5 on page 9* - Synchronization section):

- Low level < $V_{SYN\ THL}$= 0.7 V sinking 5 mA
- High level > $V_{SYN\ THH}$ = 1.2 V sourcing 0.7 mA

Figure 40. Master driving capability to synchronize the A6985F



As anticipated above, in SLAVE mode the internal oscillator operates at 250 kHz typ. but the slope compensation is dimensioned accordingly with FSW resistors so, even if the A6985F supports synchronization over the 275 kHz - 1.4 MHz frequency range, it is important to limit the switching operation around a working point close to the selected frequency (FSW resistor).

As a consequence, to guarantee the full output current capability and to prevent the subharmonic oscillations the master must limit the driving frequency range within ± 20% of the selected frequency.

A wider frequency range may generate subharmonic oscillation for duty > 50% or limit the peak current capability (see I_{PK} parameter in *Table 5 on page 9*) since the internal slope compensation signal may be saturated.

In order to guarantee the synchronization as a slave over distribution, temperature and the output load, the external clock frequency must be lower than 1.4 MHz.

7.6 Design of the power components

7.6.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depends on the ESR value so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 44

$$I_{RMS} = I_{OUT} \bullet \sqrt{\left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta}}$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering η = 1, it is equal to $I_{OUT}/2$.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 45

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMIN} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}}$$

Equation 46

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - \Delta V_{HIGHSIDE}}$$

Where ΔV_{HIGH_SIDE} and ΔV_{LOW_SIDE} are the voltage drops across the embedded switches.

The peak-to-peak voltage across the input filter can be calculated as:

Equation 47

$$V_{PP} = \frac{I_{OUT}}{C_{IN} \bullet f_{SW}} \bullet \left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta} + ESR \bullet (I_{OUT} + \Delta I_L)$$

In case of negligible ESR (MLCC capacitor) the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

Equation 48

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \bullet f_{SW}} \bullet \left(1 - \frac{D}{\eta}\right) \bullet \frac{D}{\eta}$$

Considering η = 1 this function has its maximum in D = 0.5:

Equation 49

$$C_{INMIN} = \frac{I_{OUT}}{4 \bullet V_{PPMAX} \bullet f_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% V_{IN_MAX}.

Table 13. Input capacitors

Manufacturer	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	C3225X7S1H106M	1210	10	50
	C3216X5R1H106M	1206		
Taiyo Yuden	UMK325BJ106MM-T	1210		

7.6.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple (please refer to *Section 7.6.3*). Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by *Equation 50*:

Equation 50

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \bullet T_{ON} = \frac{V_{OUT}}{L} \bullet T_{OFF}$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed $V_{OUT,}$ is obtained at maximum T_{OFF} that is at minimum duty cycle (see *Section 7.6.1: Input capacitor selection* to calculate minimum duty).

So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

Equation 51

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{LMAX}} \bullet \frac{1 - D_{MIN}}{F_{SW}}$$

where f_{SW} is the switching frequency $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 0.5 A and F_{SW} = 2 MHz the minimum inductance value to have ΔI_L = 30% of I_{OUT} is about 8.2 µH.

The peak current through the inductor is given by:

Equation 52

$$I_{L,PK} = I_{OUT} + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In *Table 14* some inductor part numbers are listed.

Table 14. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XAL40xx	2.2 to 15	5.6 to 2.8
	XAL50xx	2.2 to 22	9.2 to 3.6
	XFL40xx	2.2 to 4.7	3.7 to 2.7

7.6.3 Output capacitor selection

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). As a consequence the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

Equation 53

$$\Delta V_{OUT} = ESR \bullet \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \bullet C_{OUT} \bullet f_{SW}}$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multi layer ceramic capacitor (MLCC).

The output capacitor is important also for loop stability: it determines the main pole and the zero due to its ESR. (see *Section 6: Closing the loop on page 39* to consider its effect in the system stability).

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.25 A, f_{SW} = 2 MHz (resulting by the inductor value) and C_{OUT} = 10 µF MLCC:

Equation 54

$$\frac{\Delta V_{OUT}}{V_{OUT}} \cong \frac{1}{V_{OUT}} \bullet \frac{\Delta I_{LMAX}}{C_{OUT} \bullet f_{SW}} = \left(\frac{1}{3.3} \bullet \frac{0.25}{8 \bullet 10\mu F \bullet 2MHz} \right) = \frac{1.6mV}{3.3} = 0.05\%$$

The output capacitor value has a key role to sustain the output voltage during a steep load transient. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. In case the final application specifies high slew rate load transient, the system bandwidth must be maximized and the output capacitor has to sustain the output voltage for time response shorter than the loop response time.

In *Table 15* some capacitor series are listed.

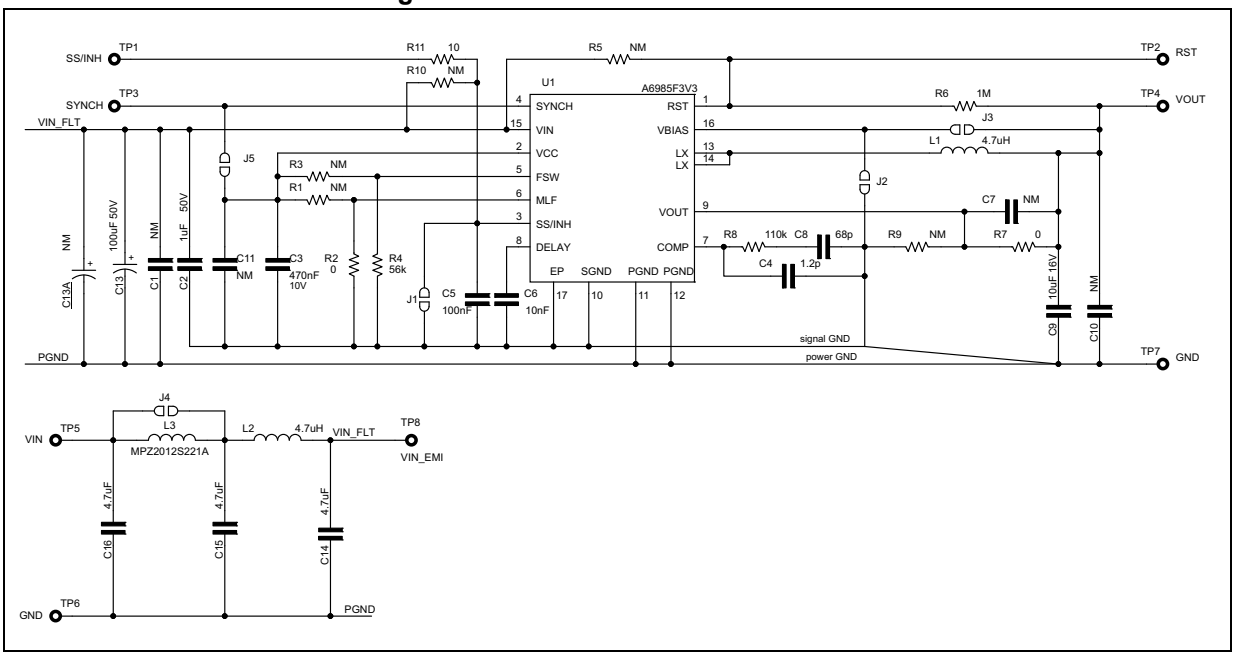
Table 15. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

8 Application board

The reference evaluation board schematic is shown in *Figure 41*.

Figure 41. Evaluation board schematic



The additional input filter (C16, L3, C15, L2, C14) limits the conducted emission on the power supply (refer to *Figure 56 on page 68*).

Table 16. Common bill of material

Reference	Part number	Description	Manufacturer
C1, C10, C11		Not mounted	
C2	C2012X7S2A105K	1 µF - 0805 - 50 V - X7S - 10%	TDK
C3		470 nF - 10 V - 0603	
C4, C7, C8		See *Table 17*, *Table 18 on page 61*, *Table 19 on page 63*	
C5		100 nF - 10 V - 0603	
C6		10 nF - 10 V - 0603	
C9	CGA5L3X5R1H106K	10 µF - 1206 - 50 V - X5R - 10%	TDK
C14, C15, C16	CGA5L3X5R1H475k	4.7 µF - 1206 - 50 V - X7R - 10%	TDK
C13	UWD1H101MCQ1GS	100 µF - 50 V - 20%	Nichicon
R2		0 Ω - 0603	
R6		1 MΩ - 1%- 0603	
R4		56 kΩ - 1% - 0603	
R7, R8, R9		See *Table 17*, *Table 18*, *Table 19*	

Table 16. Common bill of material (continued)

Reference	Part number	Description	Manufacturer
R11		10 Ω - 1% - 0603	
R1, R3, R5, R10		Not mounted	
L1	XAL4030-472MEC	4.7 µH	Coilcraft
L2	XAL4030-472MEC	4.7 µH	Coilcraft
L3	MPZ2012S221A	EMC bead	TDK
J1	Open		
J2	Open		
J3	Closed	Switchover	
J4	Open		
J5		To adjust the ISKIP current level in LCM operation. Leave open in LNM.	
U1	See *Table 17*, *Table 18*, *Table 19 on page 63*		STMicroelectronics

The layout of the board is shown in *Figure 42* and in *Figure 43*.

Figure 42. Top layer

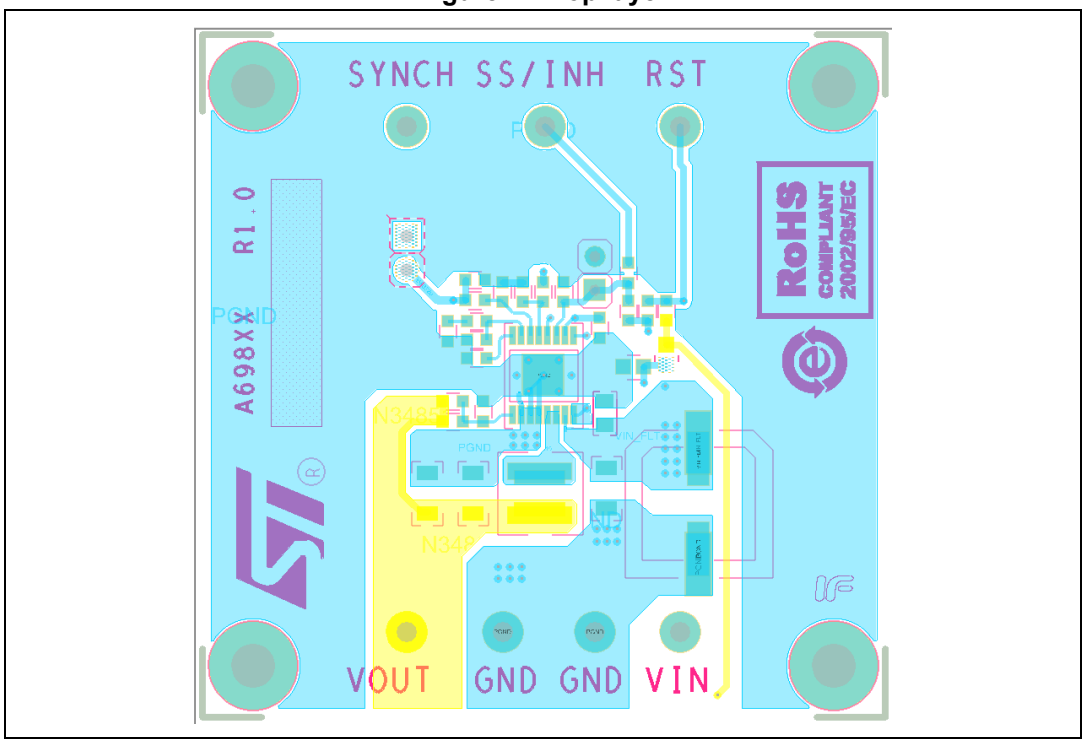
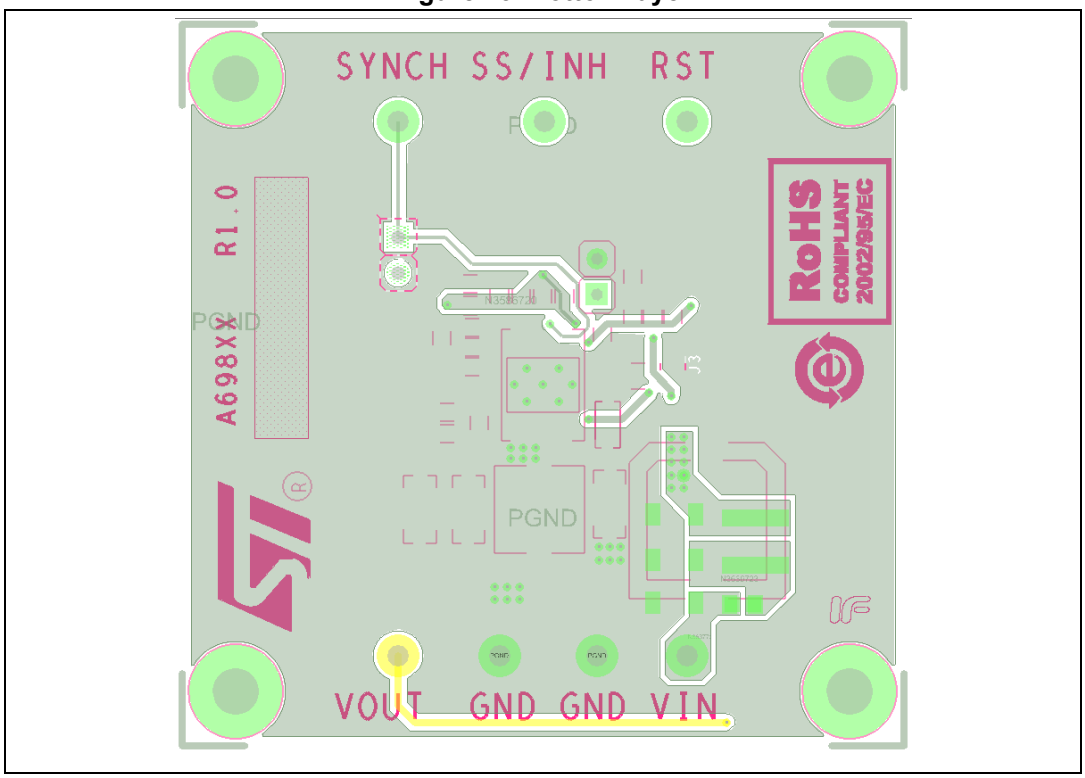


Figure 43. Bottom layer



8.1 A6985F3V3 evaluation board

Table 17. Bill of material of A6985F3V3 demonstration board

Reference	Part number	Description	Manufacturer
C4		1.2 pF - 10 V - 0603	
C7		Not mounted	
C8		68 pF - 10 V - 0603	
R7		0 Ω - 0603	
R8		110 kΩ - 1% - 0603	
R9		Not mounted	
U1	A6985F3V3		STMicroelectronics

Equation 55 and *Figure 44* show the magnitude and phase margin Bode's plots related to the evaluation board presented in *Figure 41* with the BOM of *Table 16* and *Table 17*.

The small signal dynamic performance of the demonstration board is:

Equation 55

$$BW = 110kHz$$

$$\text{phase margin} = 67^0$$

Figure 44. Magnitude Bode's plot of A6985F3V3 evaluation board

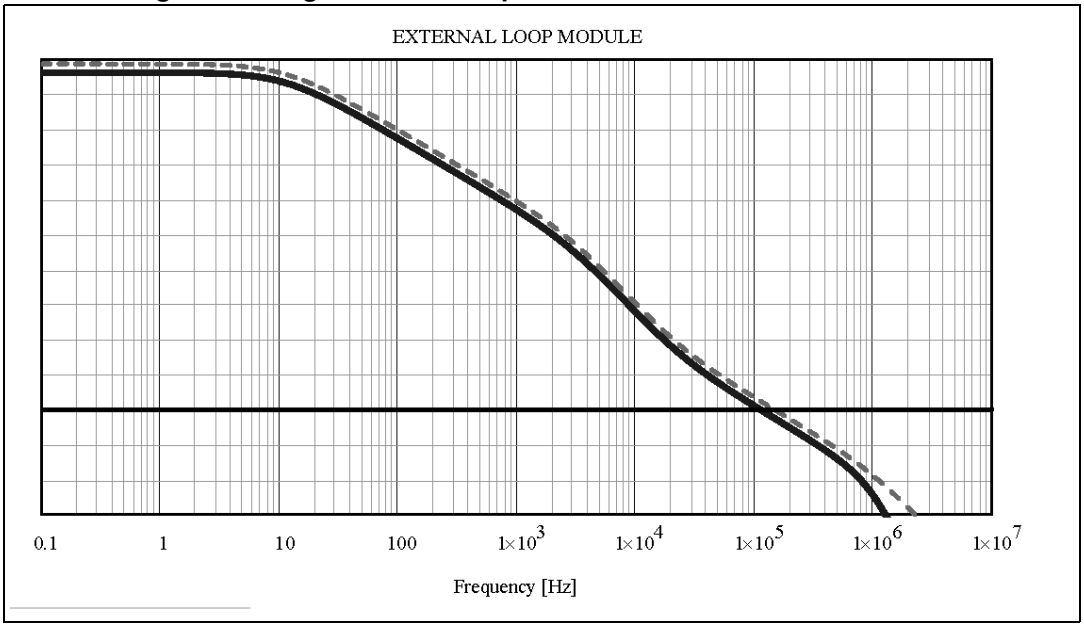
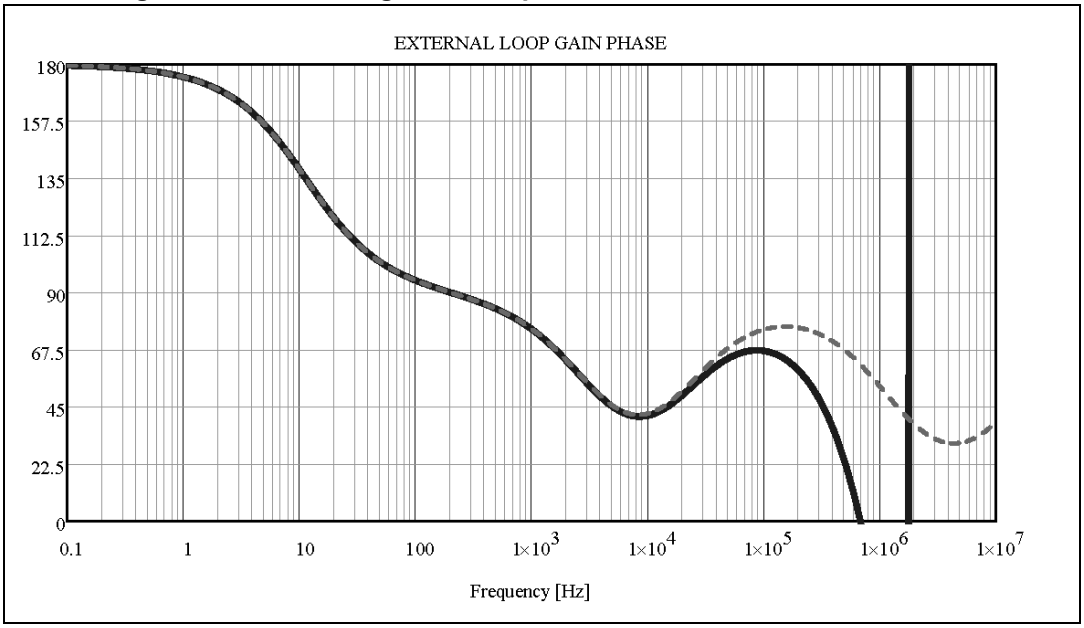


Figure 45. Phase margin Bode's plot of A6985F3V3 evaluation board



8.2 A6985F5V evaluation board

Table 18. Bill of material of A6985F5V demonstration board

Reference	Part number	Description	Manufacturer
C4		1.2 pF - 10 V - 0603	
C7		Not mounted	
C8		47 pF - 10 V - 0603	
R7		0 Ω - 0603	
R8		150 kΩ - 1% - 0603	
R9		Not mounted	
U1	A6985F5V		STMicroelectronics

Figure 46 and *Figure 47* show the magnitude and phase margin Bode's plots related to the evaluation board presented in *Figure 41 on page 57* with the BOM of *Table 16 on page 57* and *Table 18*.

The small signal dynamic performance of the demonstration board is:

Equation 56

$$BW = 100kHz$$

$$\text{phase margin} = 69^0$$

Figure 46. Magnitude Bode's plot of A6985F5V evaluation board

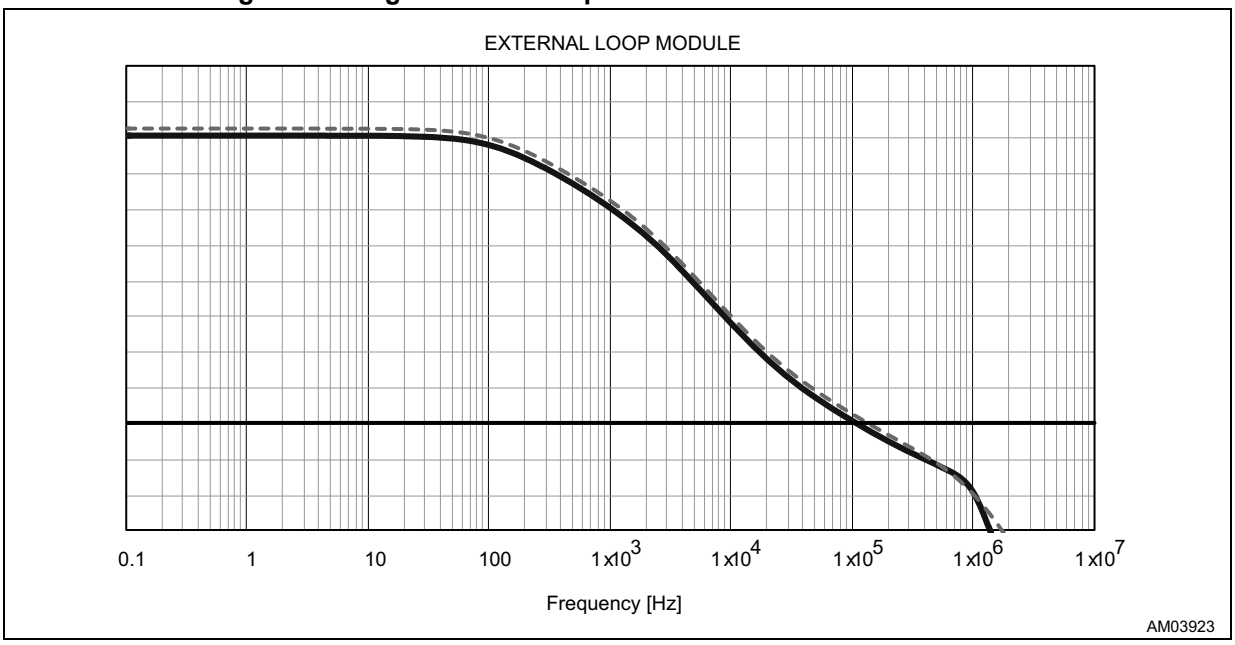
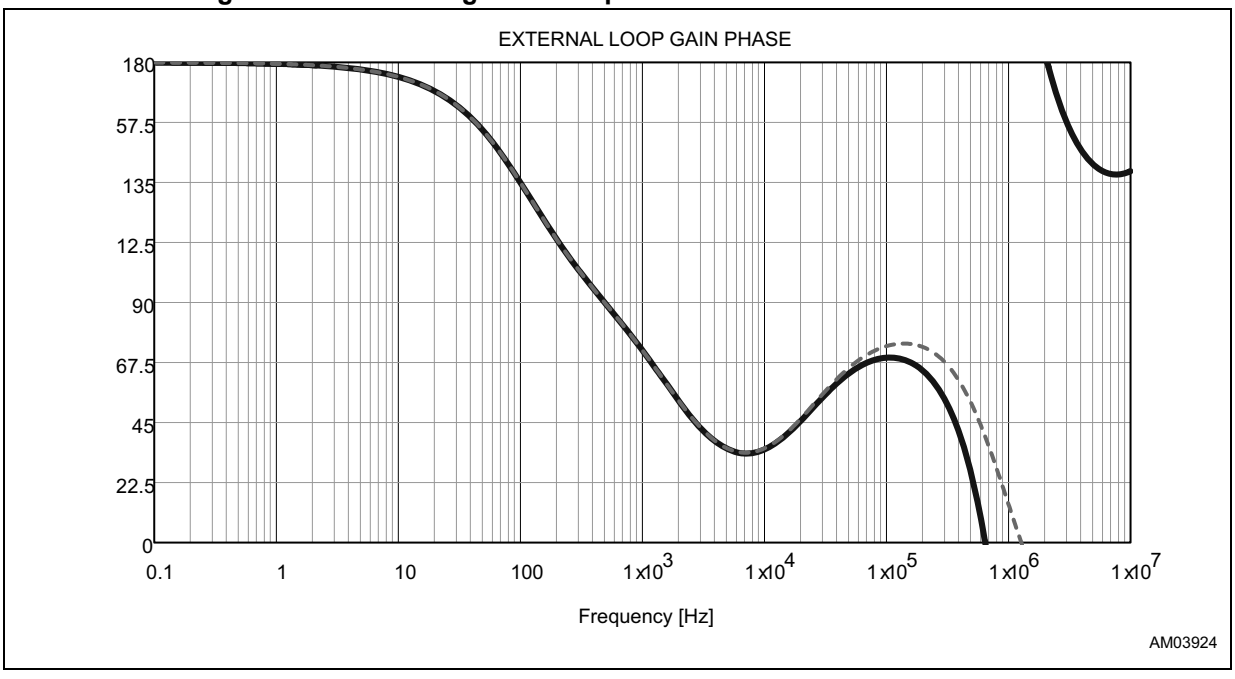


Figure 47. Phase margin Bode's plot of A6985F5V evaluation board



8.3 A6985F (V_{OUT} = 6 V) evaluation board

Table 19. Bill of material of A6985F (V_{OUT} = 6 V) demonstration board

Reference	Part number	Description	Manufacturer
C4		1.2 pF - 10 V - 0603	
C7		4.7 pF - 10 V - 0603	
C8		27 pF - 10 V - 0603	
R7		200 kΩ - 1% - 0603	
R8		200 kΩ - 1% - 0603	
R9		33 kΩ - 1% - 0603	
U1	A6985F		STMicroelectronics

Figure 48 and *Figure 49* show the magnitude and phase margin Bode's plots related to the evaluation board presented in *Figure 41 on page 57* with the BOM of *Table 16 on page 57* and *Table 19*.

The small signal dynamic performance of the demonstration board is:

Equation 57

$$BW = 110kHz$$

$$\text{phase margin} = 60^0$$

Figure 48. Magnitude Bode's plot of A6985F (V_{OUT} = 6 V) evaluation board

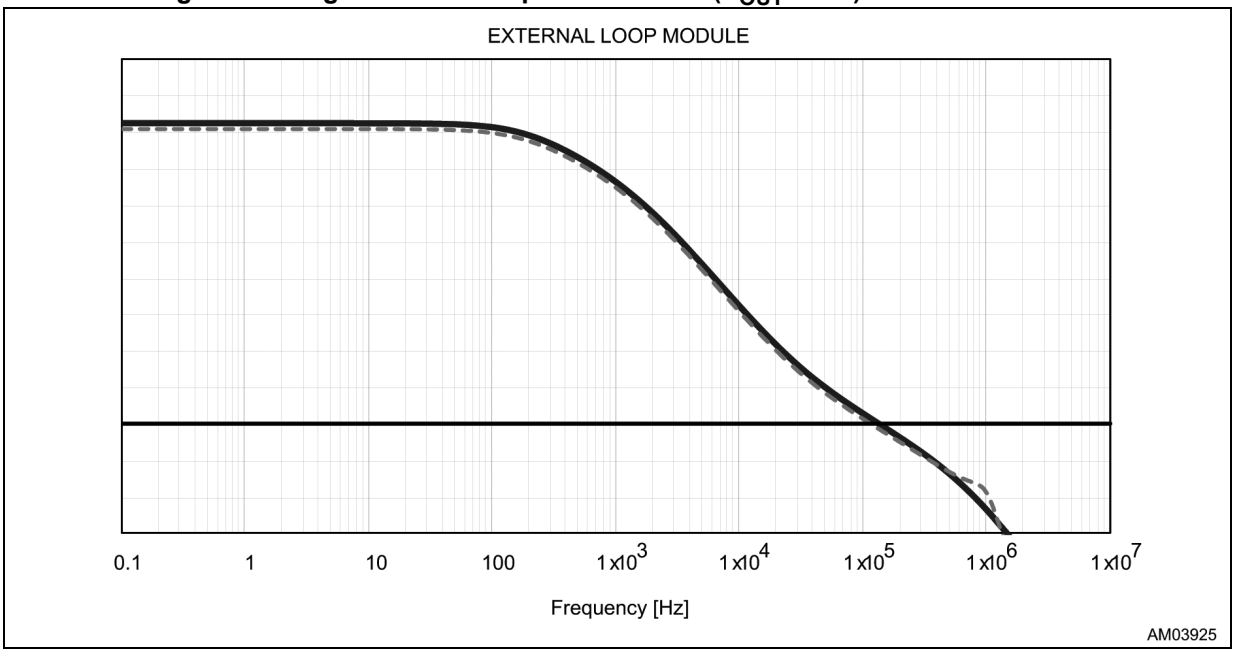
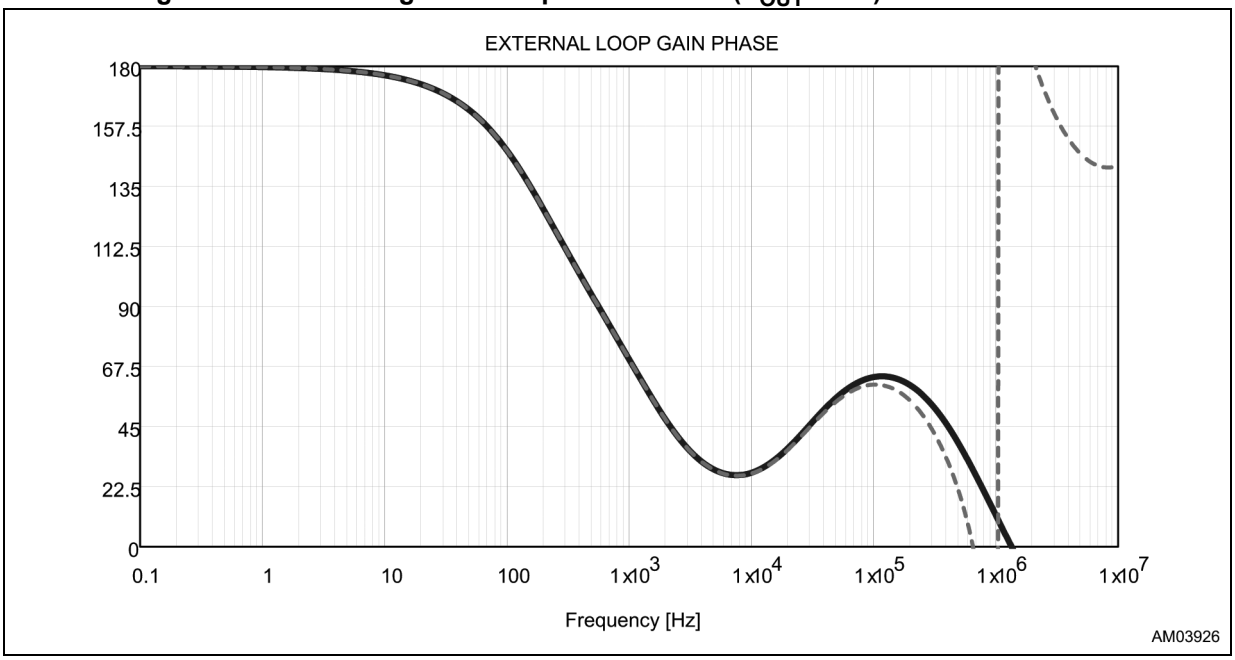


Figure 49. Phase Margin Bode's plot of A6985F (V_{OUT} = 6 V) evaluation board



9 Efficiency curves

Figure 50. A6985F3V3 efficiency curves: V_{IN} = 13.5 V - f_{sw} = 2 MHz

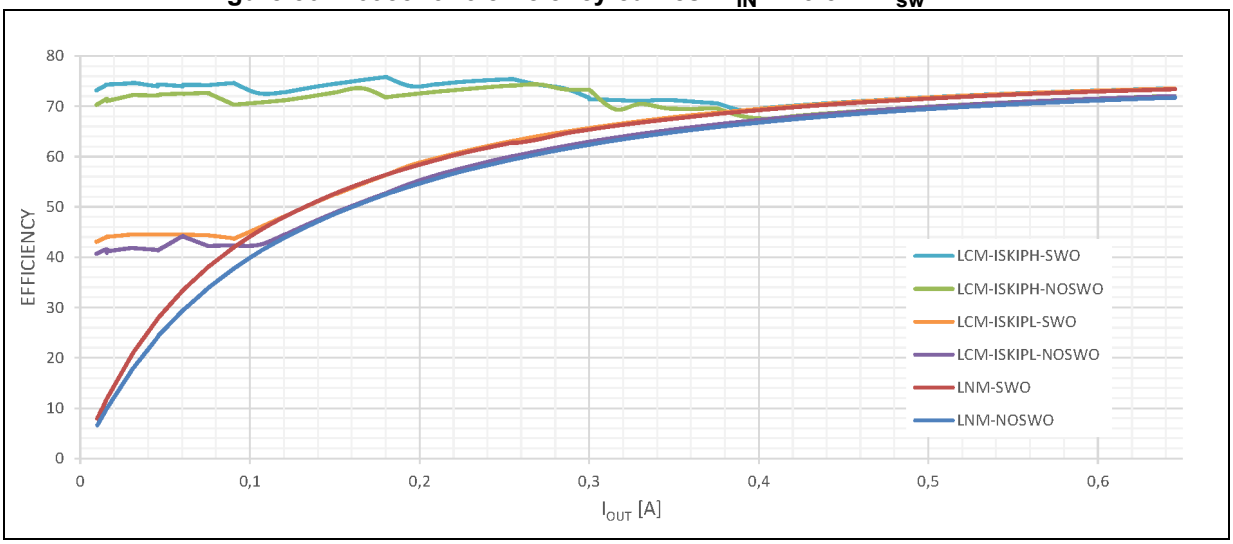


Figure 51. A6985F3V3 efficiency curves: V_{IN} = 13.5 V - f_{sw} = 2 MHz (log scale)

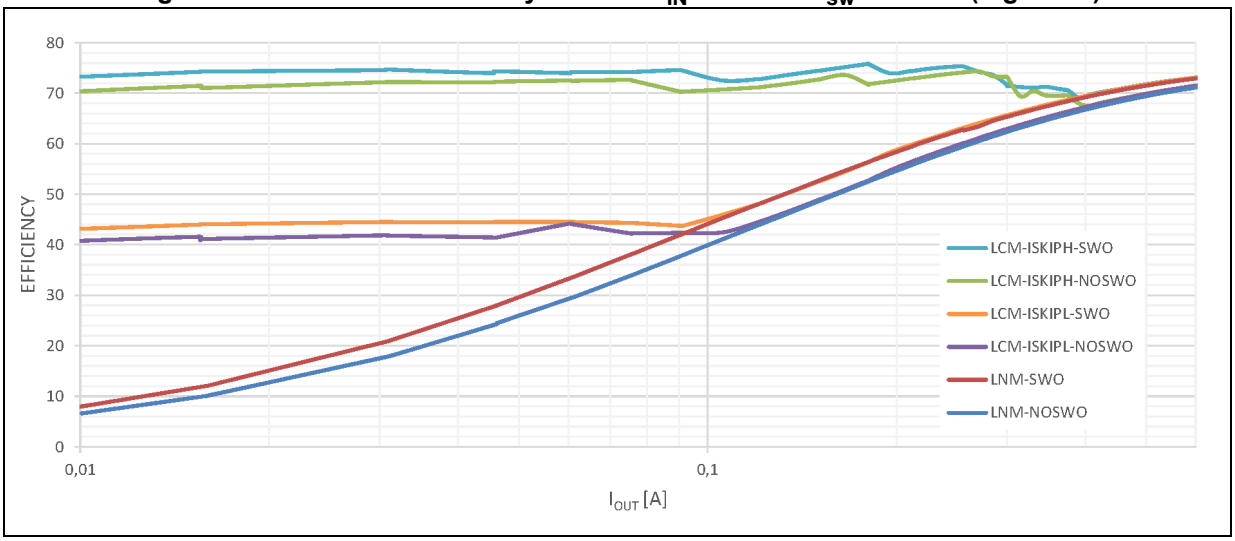


Figure 52. A6985F3V3 efficiency curves: V_{IN} = 24V - f_{sw} = 2 MHz

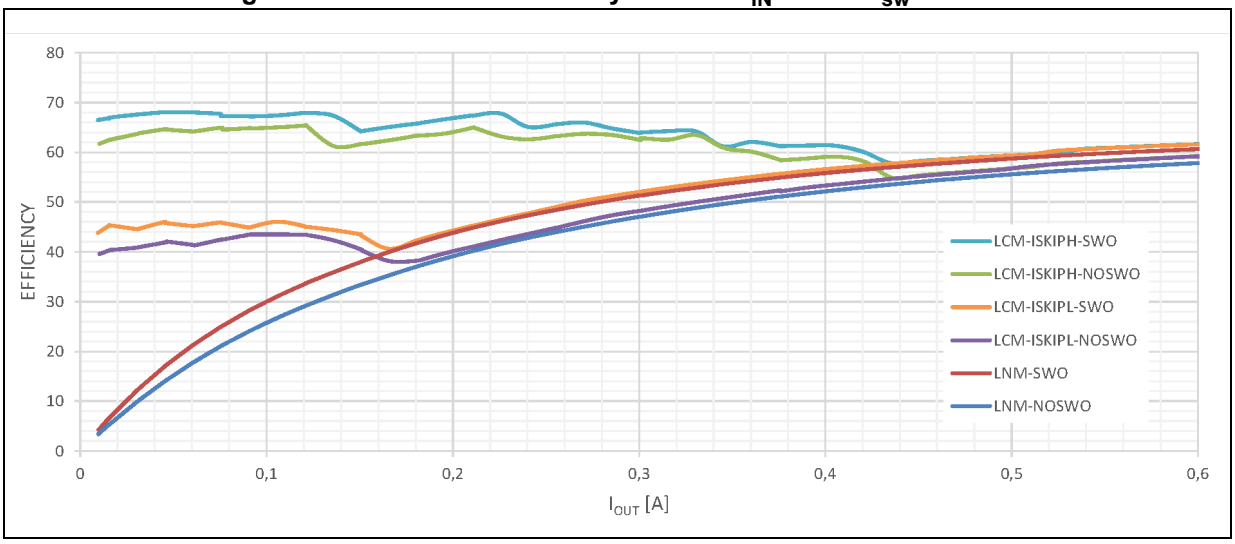


Figure 53. A6985F3V3 efficiency curves: V_{IN} = 24 V - f_{sw} = 2 MHz (log scale)

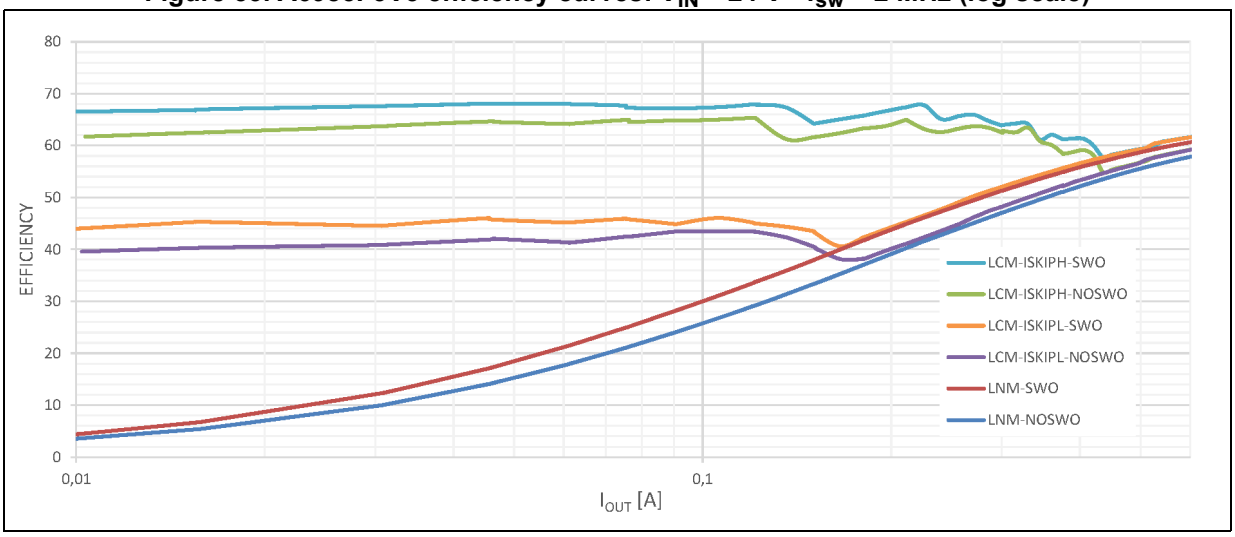


Figure 54. A6985F5V efficiency curves: V_{IN} = 13.5 V - f_{sw} = 2 MHz

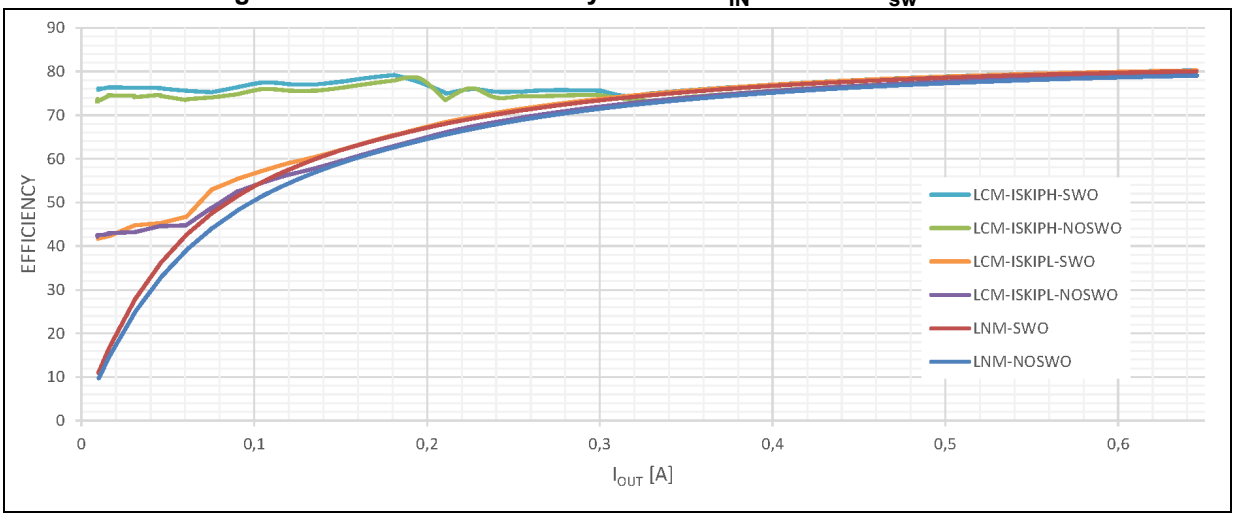


Figure 55. A6985F5V efficiency curves: V_{IN} = 13.5 V - f_{sw} = 2 MHz (log scale)

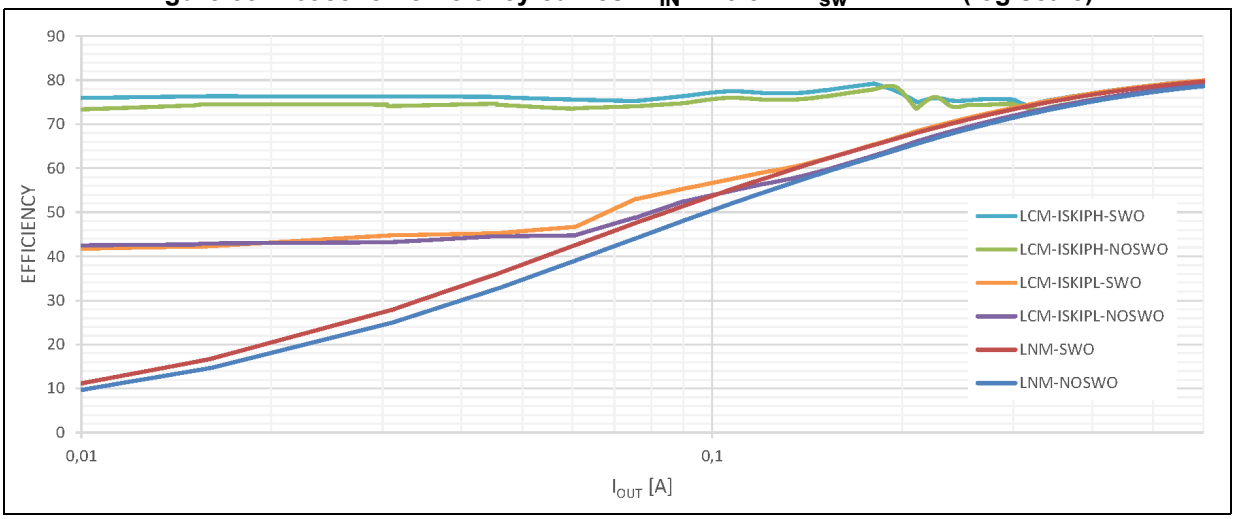


Figure 56. A6985F5V efficiency curves: V_{IN} = 24 V - f_{sw} = 2 MHz

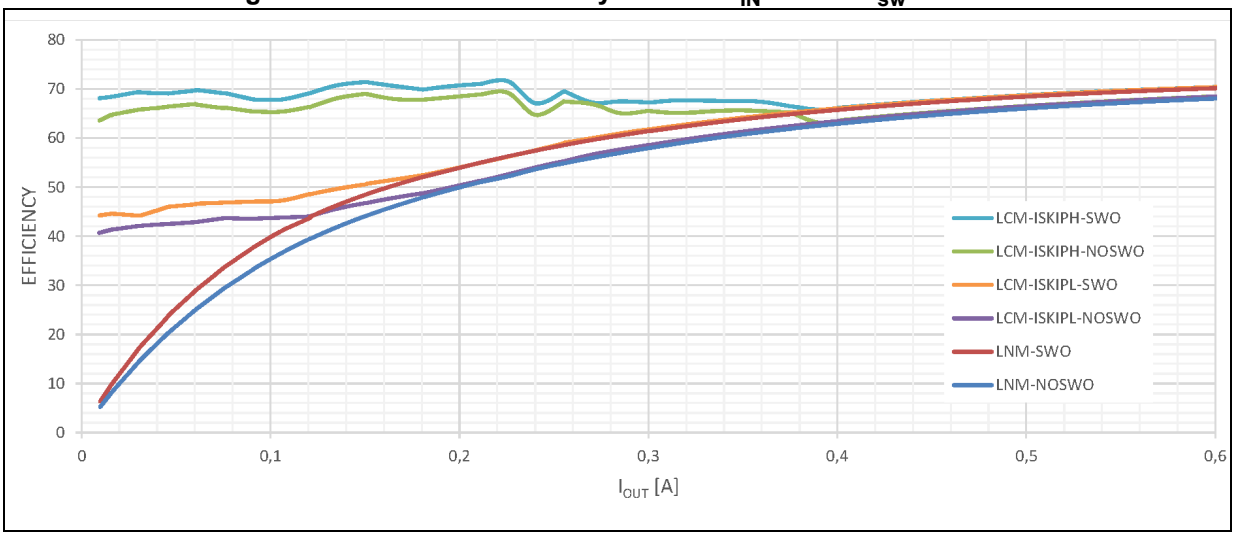
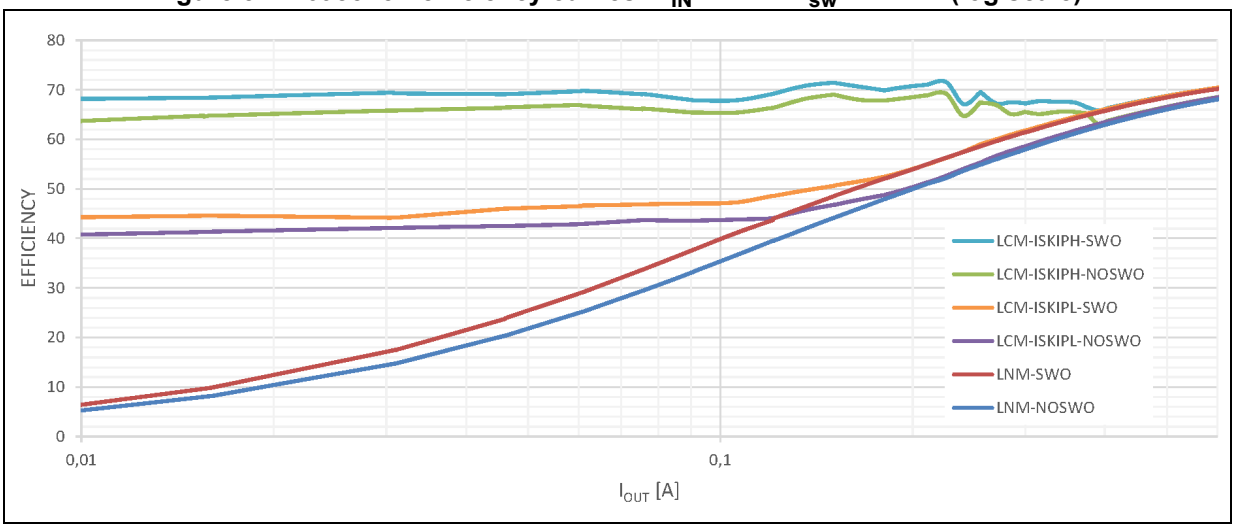


Figure 57. A6985F5V efficiency curves: V_{IN} = 24 V - f_{sw} = 2 MHz (log scale)



10 EMC testing results

This chapter reports EMC testing results for the A6985F evaluation board (see *Section 8 on page 57*) accordingly with the following test methods:

- CE 150R for conducted emission
- DP for conducted immunity

All the measurement were performed on the A6985F5V at I_{LOAD} = 10% and 75% as defined in *Table 22*.

Table 20. CE 150R test method

	Conducted emission, CE 150R	
Frequency range	150 kHz - 30 MHz	30 MHz - 1 GHz
Bandwidth	9 kHz	120 kHz
Step size	5 kHz	60 kHz
Dwell time	2 complete software cycles minimum	
Detectors	Peak + average	

Table 21. DPI test method

	Conducted Immunity, DPI						
Frequency range	10 kHz - 150 kHz	150 kHz - 1 MHz	1 MHz - 10 MHz	10 MHz - 100 MHz	100 MHz - 200 MHz	200 MHz - 400 MHz	400 MHz - 1 GHz
Step size (linear)	10 kHz	100 kHz	500 kHz	1 MHz	2 MHz	4 MHz	10 MHz
Dwell time	2 sec. but min. 2 software complete cycles						
Modulation	CW						
	AM 1 kHz, 80% (same peak value as CW)						

DPI: 30 dBm for global pins, 12 dBm for local pins.

All the pins under DPI testing (see *Table 22*) satisfy class 3 limits.

Table 22. Pin testing

Pin name	Remarks	classification	CE	DPI
VS1	Filtered VIN pin	Global	X	X
VIN	VIN pin	Global	X	X
VOUT	Regulated output voltage	Local	X	
RST	RST pin	Local	X	
SS/INH	SS/INH pin	Local	X	(X)

Figure 58 shows the schematic of the EMC board that can be configured for CE and DPI testing.

Figure 58. CE - 150R / DPI

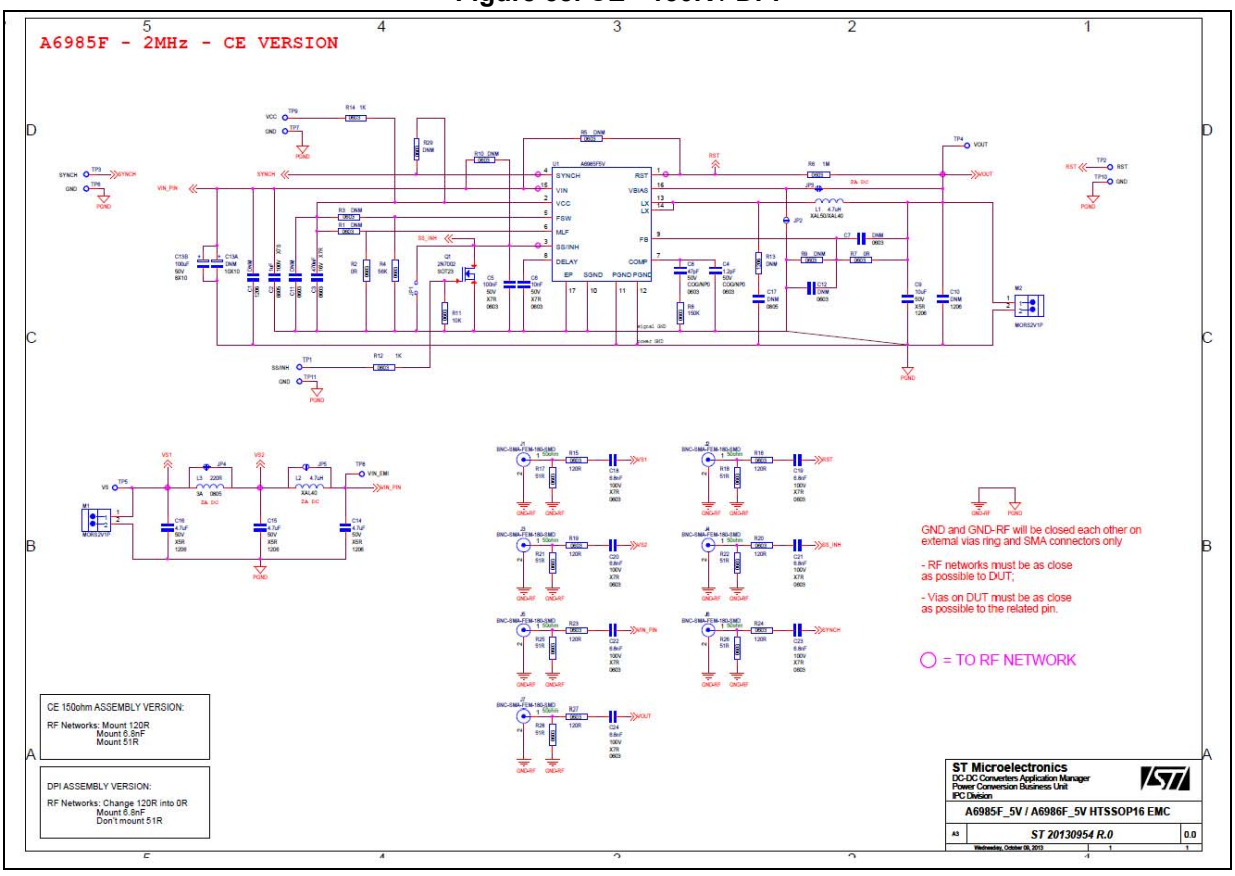


Figure 59. CE 150R at VS1 test point (see *Figure 58*) at 75% I_{LOAD}

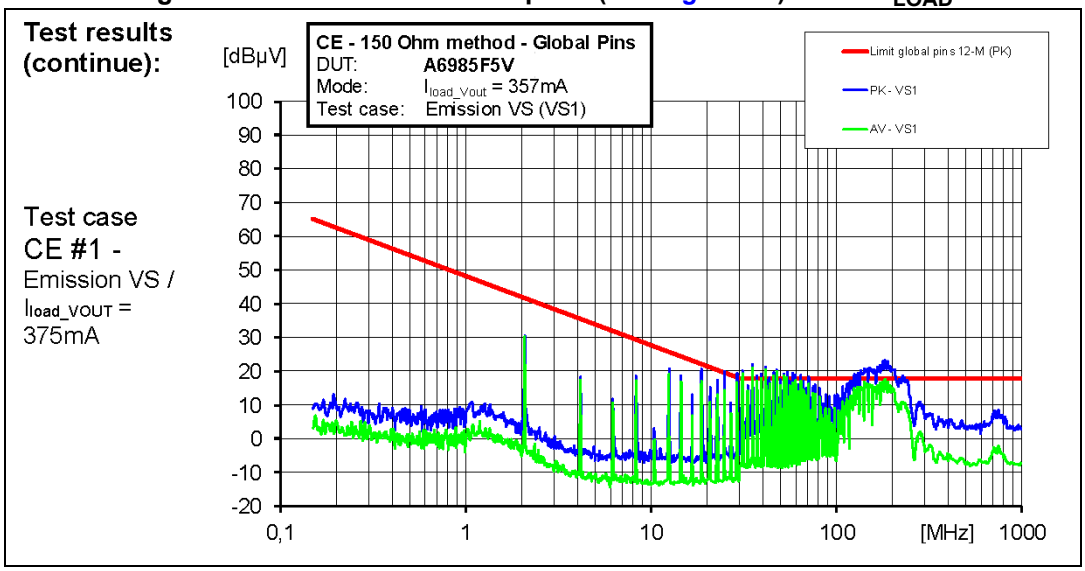


Figure 60. CE 150R at VS1 test point (see *Figure 58*) at 10% I_{LOAD}

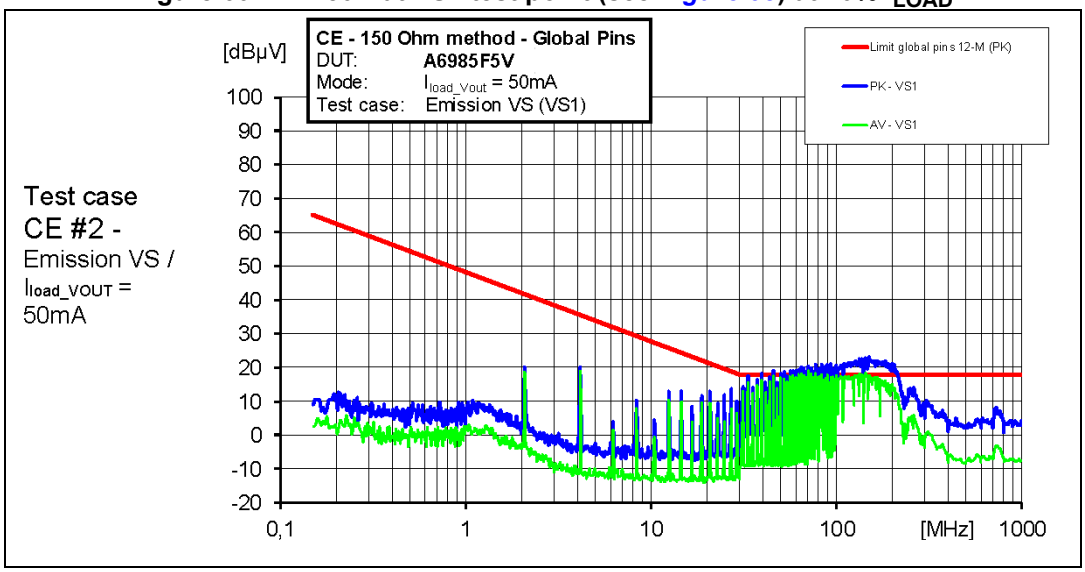


Figure 61. CE 150R at VOUT test point (see *Figure 58*) at 75% I_{LOAD}

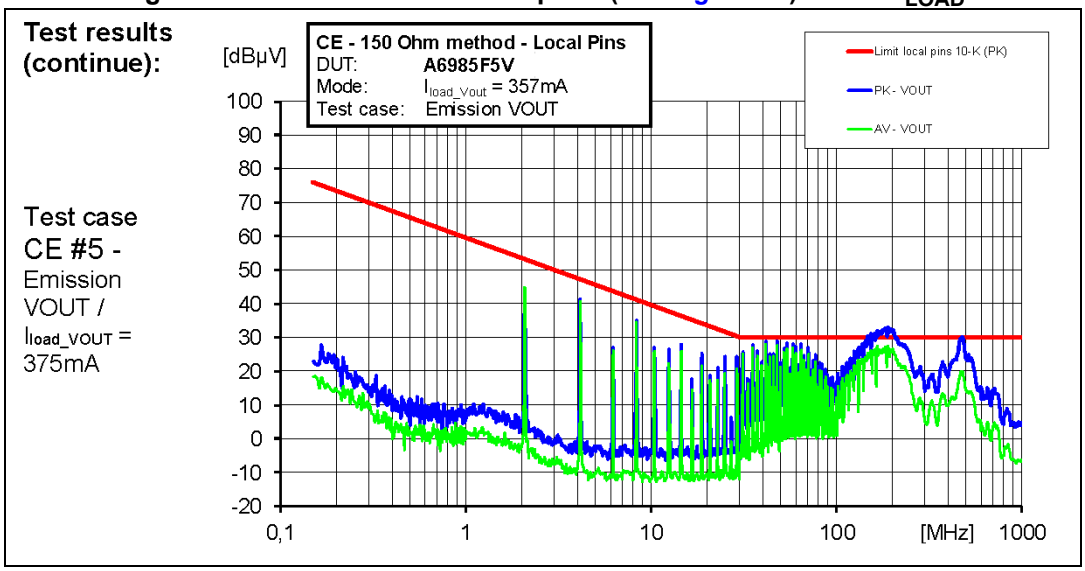


Figure 62. CE 150R at VOUT test point (see *Figure 58*) at 10% I_{LOAD}

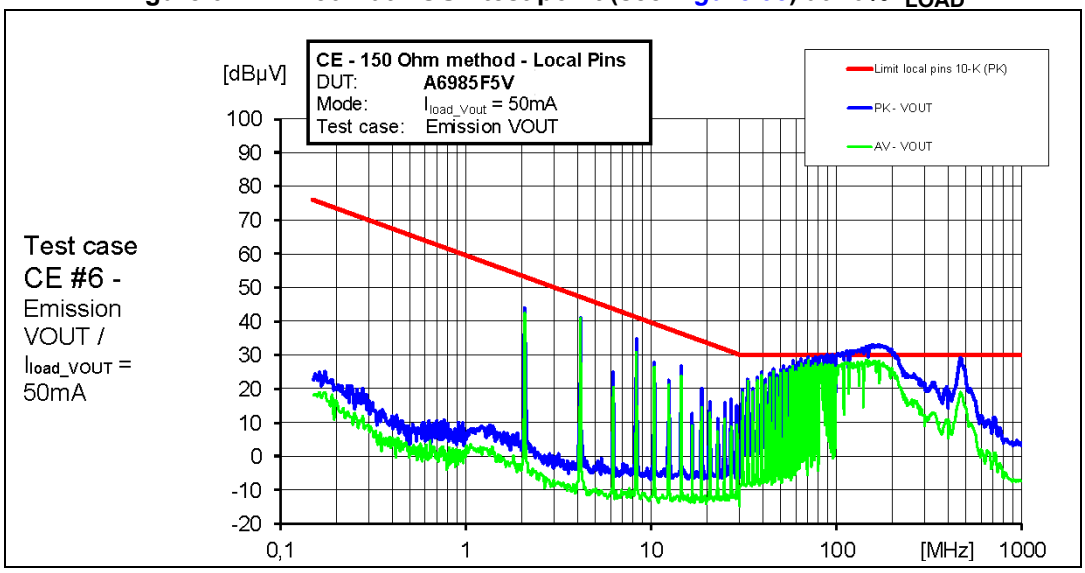


Figure 63. CE 150R at RST test point (see *Figure 58*) at 75% I_{LOAD}

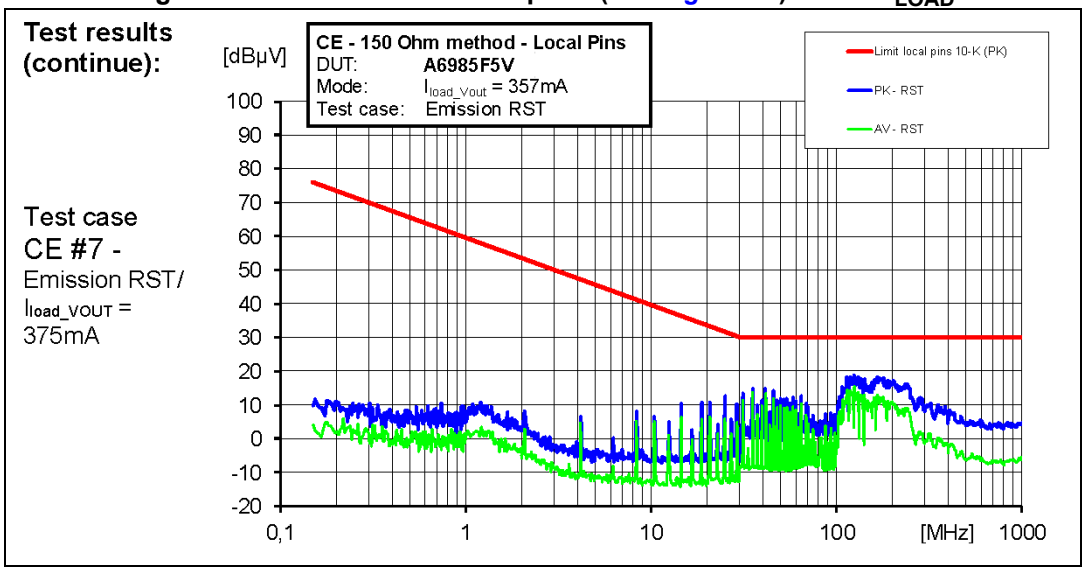


Figure 64. CE 150R at RST test point (see *Figure 58*) at 10% I_{LOAD}

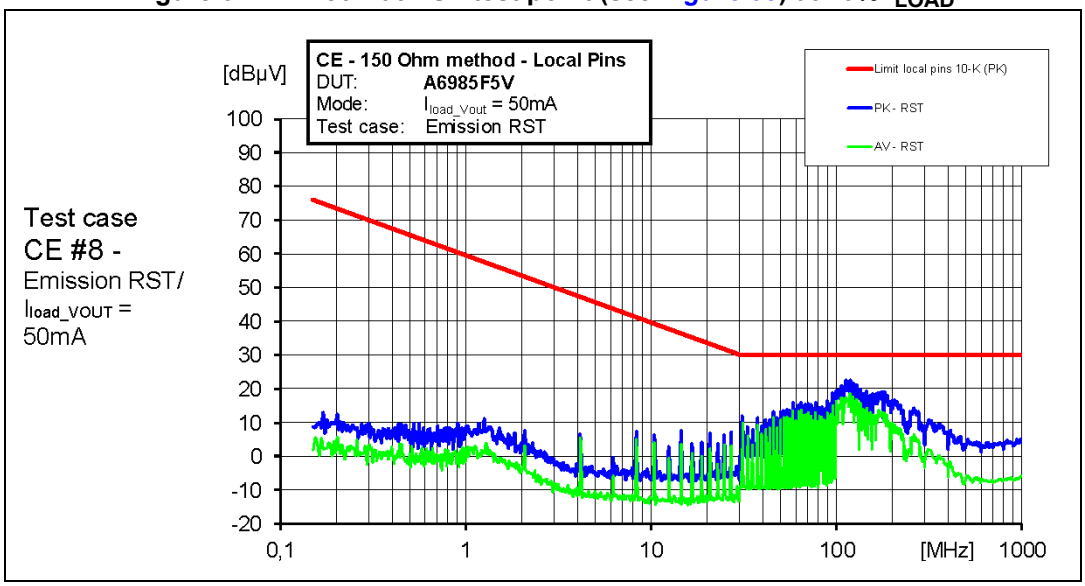


Figure 65. CE 150R at SS/INH test point (see *Figure 58 on page 70*) at 75% I_{LOAD}

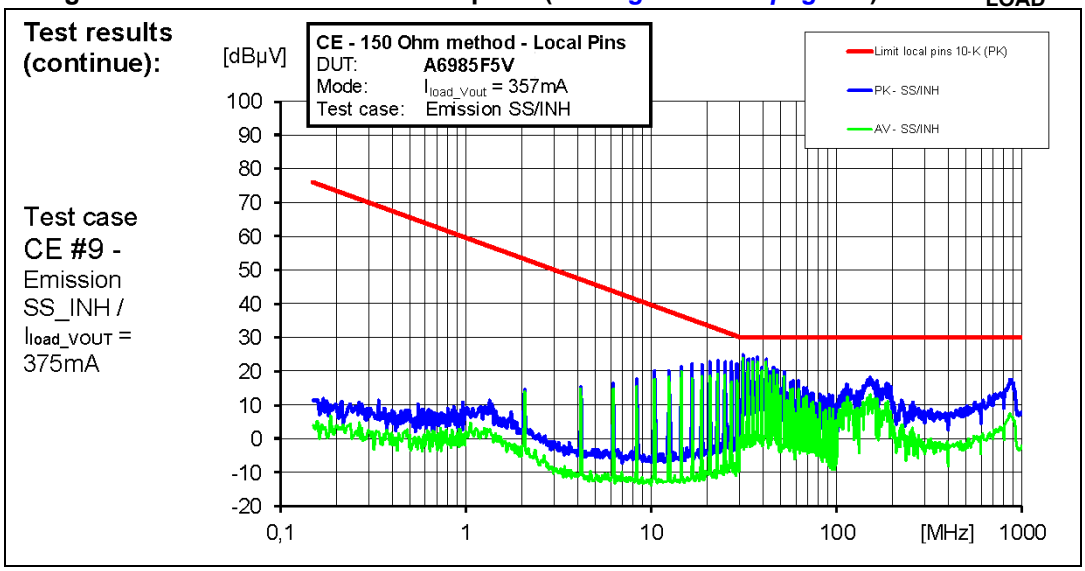
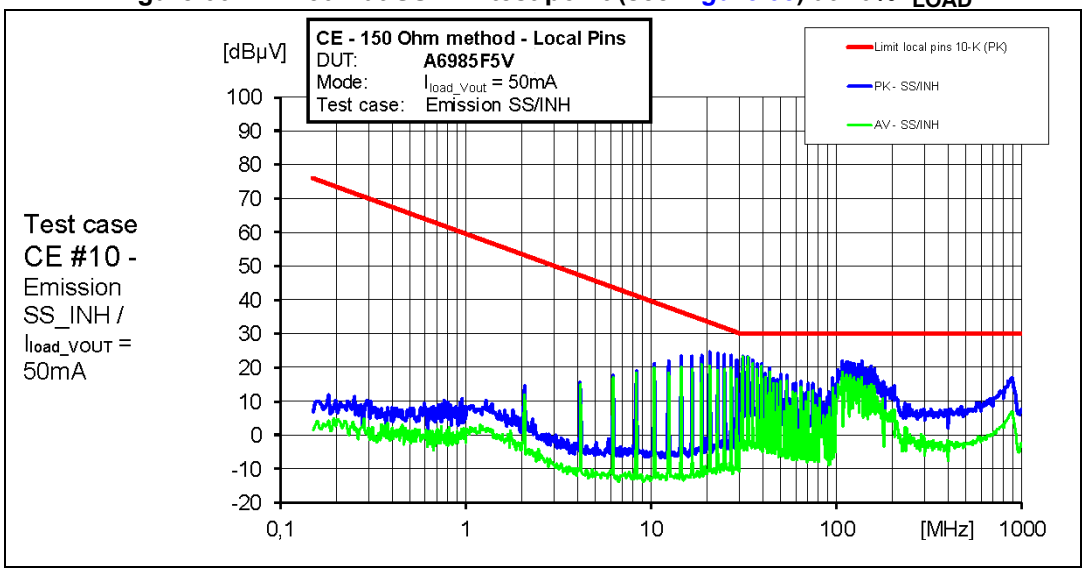


Figure 66. CE 150R at SS/INH test point (see *Figure 58*) at 10% I_{LOAD}



11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

11.1 HTSSOP16 package information

Figure 67. HTSSOP16 package outline

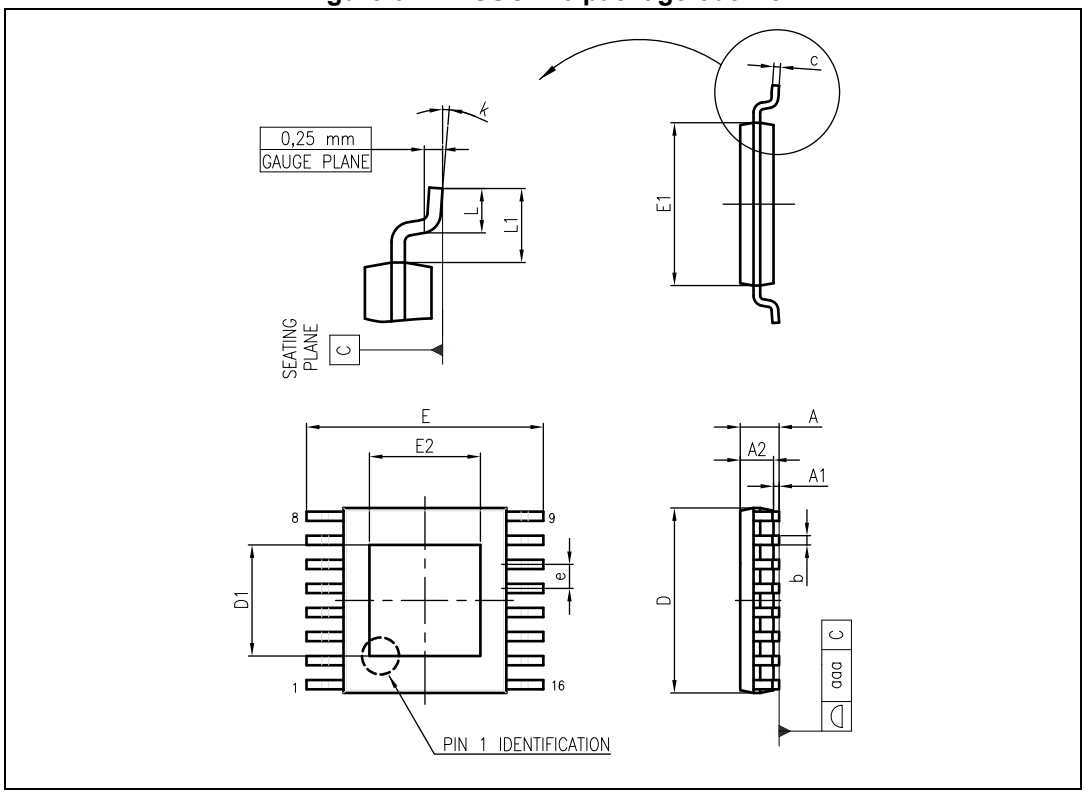


Table 23. HTSSOP16 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

12 Order codes

Table 24. Order codes

Part numbers	Package	Packaging
A6985F3V3	HTSSOP16	Tube
A6985F3V3TR		Tape and reel
A6985F5V		Tube
A6985F5VTR		Tape and reel
A6985F		Tube
A6985FTR		Tape and reel

13 Revision history

Table 25. Document revision history

Date	Revision	Changes
10-Apr-2015	1	Initial release.
15-Apr-2015	2	Updated *Table 2 on page 6* (updated V_{IN} and VOUT). Updated units below *Equation 3 on page 19* and below *Figure 33 on page 46*.
15-Feb-2016	3	Updated *Table 3: Thermal data on page 8* (added $R_{th\ JC}$). Updated *Table 6: f_{SW} selection on page 12* (added note *2.* below table). Updated *Section 7.5: Synchronization (LNM) on page 48* (replaced value of “range” “2 MHz” by “1.4 MHz”, added text).