

Precision Hall Effect Angle Sensor IC with I²C Interface

FEATURES AND BENEFITS

- 360° contactless high resolution angle position sensor
- CVH (Circular Vertical Hall) technology
- Digital I²C output
- Refresh Rate: 32 μ s, 12-bit resolution
- Automotive temperature range -40°C to 85°C
- Two types of linearization schemes offered: harmonic linearization and segmented linearization
- Linearization features enable use in off-axis applications
- EEPROM with Error Correction Control (ECC) for trimming calibration
- 1 mm thin (TSSOP-14) package
- Automatic calibration features maintain angle accuracy over airgap

DESCRIPTION

The A1332 is a 360° contactless high resolution programmable magnetic angle position sensor IC. It is designed for digital systems using an I²C interface.

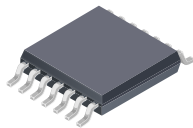
This system-on-chip (SoC) architecture includes a front end based on Circular Vertical Hall (CVH) technology, programmable microprocessor based signal processing, and digital I²C interface. Besides providing full-turn angular measurement, the A1332 also provides scaling for angle measurement applications less than 360°. It includes on-chip EEPROM technology for flexible programming of calibration parameters.

Digital signal processing functions, including temperature compensation and gain/offset trim, as well as advanced output linearization algorithms, provide an extremely accurate and linear output for both end of shaft applications, as well as off-axis applications.

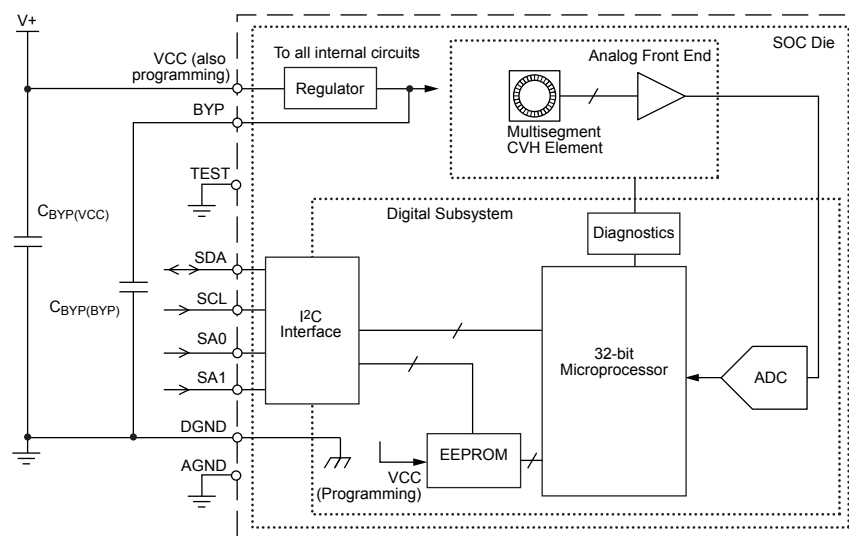
The A1332 is ideal for automotive applications requiring high speed 360° angle measurements, such as: electronic power steering (EPS), transmission, torsion bar, and other systems that require accurate measurement of angles. The A1332 linearization schemes were designed with challenging off-axis applications in mind.

The device is offered in a 14-pin TSSOP (LE) package, which has a single die. The package is lead (Pb) free, with 100% matte tin leadframe plating.

Package: 14-pin TSSOP (LE suffix)



Not to scale



Functional Block Diagram

Selection Guide

Part Number	Application	Package	Packing*	Operating Ambient Temperature, T _A
A1332ELETR-T	I ² C digital output	Single die, 14-pin TSSOP	4000 pieces per 13-in. reel	–40°C to 85°C

*Contact Allegro™ for additional packing options

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Refer to the Programming Reference addendum for information on programming the device.

SPECIFICATIONS

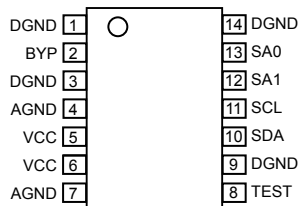
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V _{CC}		24	V
Reverse Supply Voltage	V _{RCC}		–18	V
Logic Input Voltage for I ² C Pins	V _{IN}		–0.5 to 5.5	V
Operating Ambient Temperature	T _A	E temperature range	–40 to 85	°C
Maximum Junction Temperature	T _J (max)		165	°C
Storage Temperature	T _{stg}		–65 to 170	°C

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	R _{θJA}	On 4-layer PCB based on JEDEC standard	82	°C/W

*Additional thermal information available on the Allegro website



**Package LE, 14-Pin
TSSOP Pin-out Diagram**

Terminal List Table

Pin-Name	Pin Number	Function
AGND	4, 7	Device analog ground terminal
BYP	2	Internal bypass node, connect with bypass capacitor to DGND
DGND	1, 3, 9, 14	Device digital ground terminal
SA0	13	Digital input: Sets slave address bit 0 (LSB)*; tie to BYP for 1, tie to DGND for 0
SA1	12	Digital input: Sets slave address bit 1 (LSB)*; tie to BYP for 1, tie to DGND for 0
SCL	11	Digital input: Serial clock; open drain, pull up externally to 3.3 V
SDA	10	Digital control output: digital output of evaluated target angle, also programming data input I ² C data terminal; open drain, pull up externally to 3.3 V
TEST	8	Test terminal, must be tied to DGND for correct operation
VCC	5, 6	Device power supply; also input for EEPROM writing pulse

*For additional information, refer to the Programming Reference addendum, EEPROM Description and Programming section, regarding the INTF register, I2CM field.

OPERATING CHARACTERISTICS: valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. ¹	Max.	Unit ²
Electrical Characteristics						
Supply Voltage	V _{CC}		4.5	5	5.5	V
Supply Current	I _{CC}		–	16	20	mA
VCC Low Flag Threshold ³	V _{CCLOW(TH)}		4.4	4.55	4.75	V
Supply Zener Clamp Voltage ⁶	V _{ZSUP}	I _{ZCC} = I _{CC} + 3 mA, T _A = 25°C	26.5	–	–	V
Reverse Battery Voltage	V _{RCC}	I _{RCC} = –3 mA, T _A = 25°C	–	–	–18	V
Power-On Time ^{4,5}	t _{PO}	T _A = 25°C	2	–	40	ms
I²C Interface Specification (V_{PU} = 3.3 V on SDA and SCL pins)						
Bus Free Time Between Stop and Start ⁴	t _{BUF}		1.3	–	–	μs
Hold Time Start Condition ⁴	t _{HD(STA)}		0.6	–	–	μs
Setup Time for Repeated Start Condition ⁴	t _{SU(STA)}		0.6	–	–	μs
SCL Low Time ⁴	t _{LOW}		1.3	–	–	μs
SCL High Time ⁴	t _{HIGH}		0.6	–	–	μs
Data Setup Time ⁴	t _{SU(DAT)}		100	–	–	ns
Data Hold Time ⁴	t _{HD(DAT)}		0	–	900	ns
Setup Time for Stop Condition ⁴	t _{SU(STO)}		0.6	–	–	μs
Logic Input Low Level (SDA and SCL pins) ⁶	V _{IL(I2C)}	T _A = 25°C	–	–	0.9	V
Logic Input High Level (SDA and SCL pins) ⁶	V _{IH(I2C)}	T _A = 25°C	2.1	–	3.63	V
Logic Input Current ⁶	I _{IN}	V _{IN} = 0 V to V _{CC} , T _A = 25°C	–1	–	1	μA
Output Voltage (SDA pin) ⁶	V _{OL(I2C)}	R _{PU} = 1 kΩ, C _B = 100 pF, T _A = 25°C	–	–	0.6	V
Logic Input Rise Time (SDA and SCL pins) ⁴	t _{r(IN)}		–	–	300	ns
Logic Input Fall time (SDA and SCL pins) ⁴	t _{f(IN)}		–	–	300	ns
SDA Output Rise Time ⁴	t _{r(OUT)}	R _{PU} = 1 kΩ, C _B = 100 pF	–	–	300	ns
SDA Output Fall Time ⁴	t _{f(OUT)}	R _{PU} = 1 kΩ, C _B = 100 pF	–	–	300	ns
SCL Clock Frequency ⁶	f _{CLK}	T _A = 25°C	–	–	400	kHz
SDA and SCL Bus Pull-Up Resistor	R _{PU}		–	1	–	kΩ
Total Capacitive Load for Each of SDA and SCL buses ⁶	C _B	T _A = 25°C	–	–	100	pF
Pull-Up Voltage	V _{PU}	R _{PU} = 1 kΩ, C _B = 100 pF	2.97	3.3	3.63	V

¹Typical data is at T_A = 25°C and V_{CC} = 5 V and it is for design information only.

²1 G (gauss) = 0.1 mT (millitesla).

³VCC Low Threshold Flag will be sent via the I²C interface as part of the angle measurement. When V_{CC} goes below the minimum value of V_{CCLOW(TH)}, the VCC Low Flag is set. See programming manual for details.

⁴Min. and Max. parameters for this characteristic are determined by design. They are not measured at final test.

⁵End user can customize what power-on tests are conducted at each power-on that causes a wide range of power-on times. For more information, see the description of the CFG register, which is available in the programming manual.

⁶This Parameter is tested at wafer probe only.

Continued on the next page...

OPERATING CHARACTERISTICS (continued): valid throughout full operating voltage and ambient temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. ¹	Max.	Unit ²
Magnetic Characteristics						
Magnetic Field ⁹	B	Range of input field	300	–	1000	G
Angle Characteristics						
Output ¹⁰	RES _{ANGLE}		–	12	–	bits
Effective resolution ¹¹		B = 300 G, T _A = 25°C, ORATE = 0	–	10.1	–	bits
Angle Refresh Rate ¹²	t _{ANG}	ORATE = 0	–	32	–	μs
Response Time ¹³	t _{RESPONSE}	All linearization and computations disabled, see figure 1, note 12	–	68	–	μs
Angle Error		T _A = 25 to 85°C, ideal magnet alignment, B = 300 G, target rpm = 0, no linearization	–2	–	2	deg.
Angle Noise ^{14,15}	N _{ANG3Σ}	T _A = 25°C, 30 samples, B = 300 G, no internal filtering.	–	0.6	–	deg.
		T _A = 85°C, 30 samples, B = 300 G, no internal filtering	–	0.8	–	deg.
Temperature Drift	ANGLE _{DRIFT}	T _A = –40°C, B = 300 G, drift measured relative to T _A = 25°C	–2	–	2	deg.
		T _A = 85°C, B = 300 G, drift measured relative to T _A = 25°C	–1.5	–	1.5	deg.
Angle Drift over Life-Time ¹⁶	ANGLE _{DRIFT-LIFE}	B = 300G, drift observed after AEC-Q100 qualification testing	–	±1	–	deg.

⁷Typical data is at T_A = 25°C and V_{CC} = 5 V and it is for design information only.

⁸1 G (gauss) = 0.1 mT (millitesla).

⁹This represents a typical input range.

¹⁰RES_{ANGLE} represents the number of bits of data available for reading from the device registers.

¹¹Effective Resolution is calculated using the formula below:

$$\log_2(360) - \log_2\left(3 \times \sum_{l=1}^{32} \sigma_l\right)$$

where σ is the Standard Deviation based on thirty measurements taken at each of the 32 angular positions, $l = 11.25, 22.5, \dots, 360$.

¹²The rate at which a new angle reading is ready. This value varies with the ORATE selection.

¹³This value assumes no linearization, (harmonic, or segmented), no IIR or ORATE filtering, and no short-stroke features enabled. This number also does not account for the added latency associated with the I2C interface sampling rate. This value only represents the time to read the magnetic position with no further computations made. Actual response time is dependent on EEPROM settings. Settings related to filter design, signal path computations, and linearization will increase the response time.

¹⁴Error and noise values are with no further signal processing. Angle Error can be corrected with linearization algorithm, and Angle Noise can be reduced with internal filtering and slower Angle Refresh Rate value. The parameters are characterized, but not measured at final test.

¹⁵This value represents 3-sigma or thrice the standard deviation of the measured samples.

¹⁶The Angle Error of most devices tested did not shift appreciably after AEC-Q100 qualification testing. However, the Angle Error of some devices was observed to drift by approximately 2 degrees after AEC-Q100 (grade 1) testing.

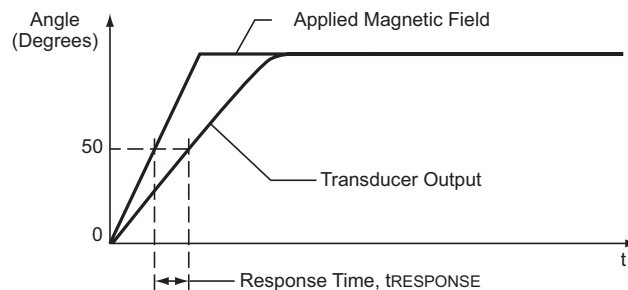


Figure 1: Definition of Response Time

FUNCTIONAL DESCRIPTION

Overview

The A1332 incorporates a Hall sensor IC that measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device). The A1332 computes the angle based on the actual physical reading, as well as any internal parameters that have been set by the user. The end user can configure the output dynamic range, output scaling, and filtering.

This device is an advanced, programmable internal microprocessor-driven system-on-chip (SoC). It includes a Circular Vertical Hall (CVH) analog front end, a high speed sampling A-to-D converter, digital filtering, a 32-bit custom microprocessor, a digital control I²C interface, and digital output of processed angle data.

Advanced linearization, offset, and gain adjustment options are available in the A1332. These options can be configured in onboard EEPROM providing a wide range of sensing solutions in the same device. Device performance can be optimized by enabling individual functions or disabling them in EEPROM to minimize latency.

Operation

The device is designed to acquire angular position data by sampling a rotating bipolar magnetic target using a multi-segmented circular vertical Hall effect (CVH) detector. The analog output is processed, and then digitized, and compensated before being loaded into the output register. Refer to figure 2 for a depiction of the signal process flow described here.

• **Analog Front End** In this stage, the applied magnetic signal is detected and digitized for more advanced processing.

A1 CVH Element. The CVH is the actual magnetic sensing element that measures the direction of the applied magnetic vector.

A2 Analog Signal Conditioning. The signal acquired by the CVH is sampled.

A3 A to D Converter. The analog signal is digitized and handed off to the Digital Front End stage.

• **Digital Front End** In this preprocessing stage, the digitized signal is conditioned for analysis.

D1 Digital Signal Conditioning. The digitized signal is decimated and band pass filtered.

D2 Raw Angle Computation. For each sample, the raw angle value is calculated.

• **Microprocessor** The preprocess signal is subjected to various standard and user-selected computations. The type and selection of computations used involves a trade-off between precision and increased response time in producing the final output.

P1 Angle Averaging. The raw angle data is received in a periodic stream (every 32 μs), and several samples are accumulated and averaged, based on user selected output rate. This feature increases the effective resolution of the system. The amount of averaging is determined by the user-programmable ORATE (output rate) field. The user can configure the quantity of averaged samples by powers of two to determine the *refresh rate*, the rate at which successive averaged angle values are fed into the post processing stages. The available rates are set as follows:

ORATE [2:0]	Quantity of Samples Averaged	Refresh Rate (μs)
000	1	32
001	2	64
010	4	128
011	8	256
100	16	512
101	32	1024
110	64	2048
111	128	4096

P1a IIR Filter (Optional) The optional IIR filter can provide more advanced multi-order filtering of the input signal. Filter coefficients can be user-programmed, and the FI bit can be programmed by the user to enable or disable this feature.

P1b Angle Compensation over Temperature and Magnetic Field (Optional) The A1332 is capable of compensating for drift in angle readings that result from changes in the device temperature through the operating ambient temperature range. The device comes from the factory pre-programmed with coefficient settings to allow compensation of linear shifts of angle with temperature. The TC bit can be programmed by the user to enable or disable this feature. The default value from Allegro factory is “enabled”. Please note, this bit must be set, to meet specifications on angle error related items in the data-sheet.

P1c Prelinearization 0 Offset (Optional, but required if linearization used.) The expected angle values should be distributed throughout the input dynamic range to optimize angle post-

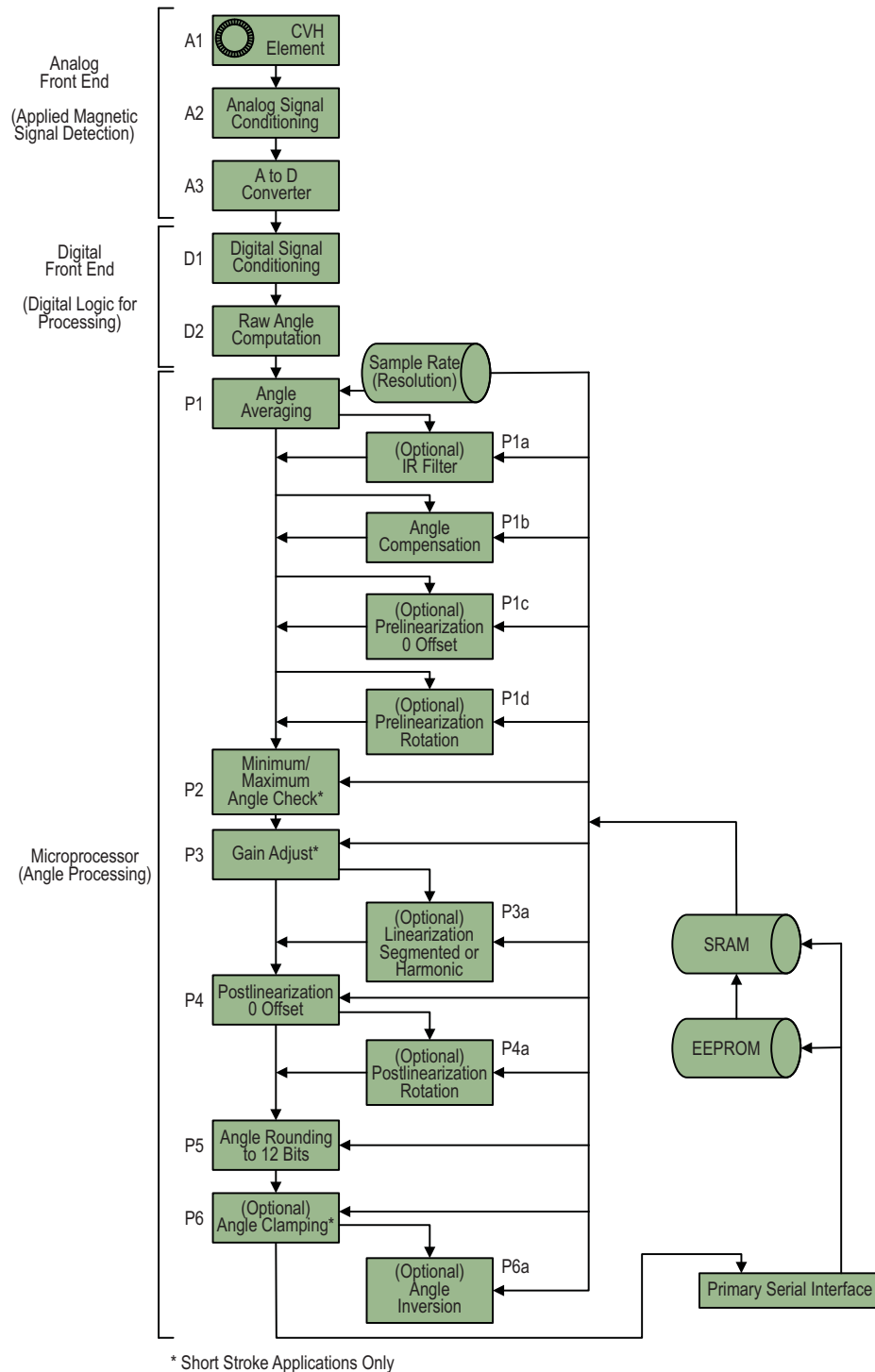


Figure 2: Signal Processing Flow
(refer by index number to text descriptions)

processing. This is mostly needed for applications that utilize full 360-degree rotations. This value establishes the position that will correspond to zero error. This value should be set such that the 360 → 0 degree range corresponds to the 4095 → 0 code range. Setting this point is critical if linearization is used, whether segmented or harmonic. This is required, prior to going through linearization, because both linearization methods require a continuous input function to operate correctly. Set using the LIN_OFFSET field.

P1d Prelinearization Rotation (Optional, but required if linearization used). The linearization algorithms require input functions that are both continuous and monotonically increasing. The LR bit sets which relative direction of target rotation results in an increasing angle value. The bit must be set such that the input to the linearization algorithm is increasing.

P2 Minimum/Maximum Angle Check. The device compares the raw angle value to the angle value boundaries set by the user programming the MIN_ANGLE_S or MAX_ANGLE_S fields. If the angle is excessive, an error flag is set at ERR[AH] (high boundary violation) or ERR[AL] (low boundary violation). (Note: To bypass this feature, set MIN_ANGLE_S to 0 and MAX_ANGLE_S to 4095.)

P3 Gain Adjust. This bit adjusts the output dynamic range of the device. For example, if the application only requires 45 degrees of stroke, the user can set this field (to 8 in this example) such that a 45-degree angular change would be distributed across the entire 4095 → 0 code range. Set using the GAIN field.

P3a Linearization (Optional). Applies user-programmed error correction coefficients (set in the LINC registers) to the raw angle measurements. Use the HL bit to enable harmonic linearization and the SL bit to enable segmented linearization (along with the LIN_SEL field to select the type of segmented linearization).

P4 Postlinearization 0 Offset. This computation assigns the final angle offset value, to set the low expected angle value to code 0 in the output dynamic range, after all linearization and processing has been completed. Set using the ZERO_OFFSET field.

P4a Postlinearization Rotation (Optional). This feature allows

the user to choose the polarity of the final angle output, relative to the result of the Prelinearization Rotation direction setting (LR bit, described above). Set using the RO bit.

P5 Angle Rounding to 12 Bits. All of the internal calculations for angle processing in the A1332 take place with 16-bit precision. This step truncates the data into a 12 bit word for output through the Primary Serial Interface.

P6 Angle Clamping. The A1332 has the ability to apply digital clamps to the output signal. This feature is most useful for applications that use angle strokes less than 360 degrees. If the output signal exceeds the upper clamp, the output will stay at the clamped value. If the output signal is lower than the lower clamp, the output will stay at the low clamp value. Set using the CLAMP_HI and CLAMP_LO fields. (Note: To bypass this feature, set CLAMP_HI to 4095 and CLAMP_LO to 0.)

P6a Angle Inversion (Optional). This calculation subtracts the angle from the high clamp.

Diagnostic Features

The A1332 features several diagnostic features and status flags to let the user know if any issues are present with the A1332 or associated magnetic system:

Condition	Diagnostic Response
$V_{CC} < V_{CCLOW(TH)(min)}$	UV error flag is set
$V_{CC} > 8.8\text{ V}$	OV error flag is set
Field > MAG_HIGH	MH flag is set
Field < MAG_LOW	ML flag is set
Angle processing errors	AT flag is set
Angle out of range	AHF, ALF flags are set
System status	ALIVE always counting indicating angles being processed

The SDA pin state changes according to the state of the VCC ramp, as shown in Figure 3.

For more information on diagnostic features and flags, please refer to the programmers guide for a more complete description of the available flags and settings.

Programming Modes

The EEPROM can be written through the primary serial interface to enter process coefficients and select options. Certain operating commands also are available by writing directly to SRAM. The EEPROM and SRAM provide parallel data structures for operating parameters. The SRAM provides a rapid test and measurement environment for application development and bench testing. The EEPROM provides persistent storage at end of line for final parameters. At initialization, the EEPROM contents are read into

the corresponding SRAM. The SRAM can be overwritten during operation (although it is not recommended). the EEPROM is permanently locked by setting the lock EEPROM [LE] bit in the EEPROM.

The A1332 is programmed through the primary serial interface, an I²C interface receiving pulses through the SDA and SCL pins, with additional power provided by pulses on the VCC pin to set the EEPROM bit fields.

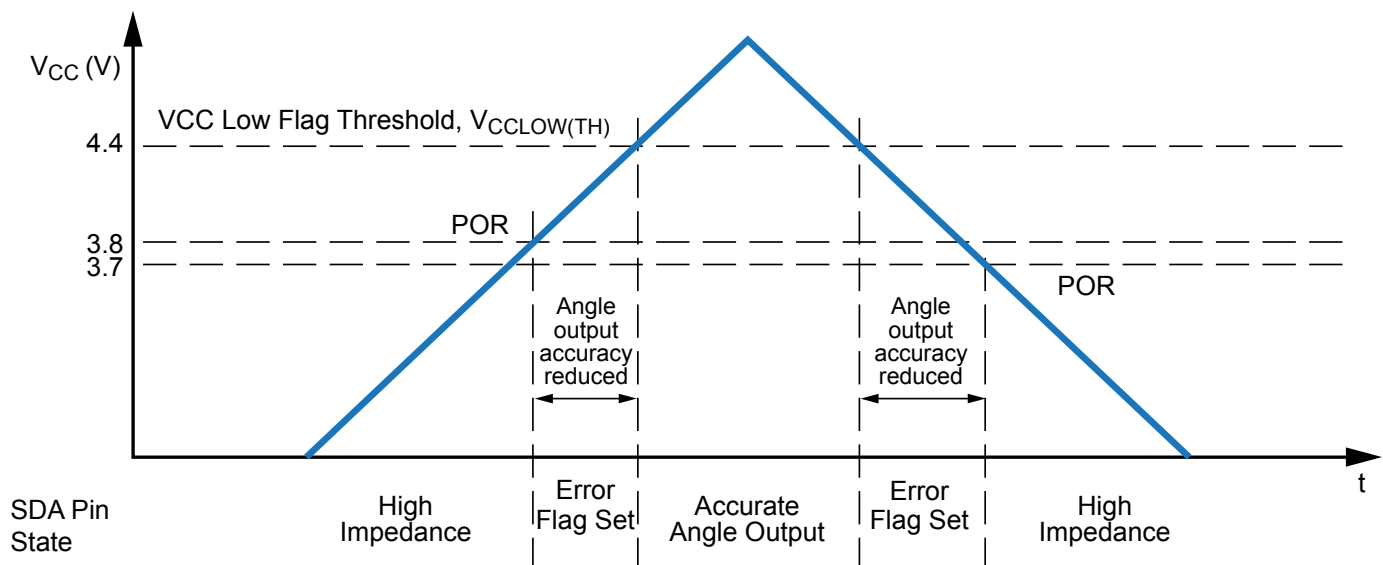


Figure 3: Relationship of VCC and SDA output

APPLICATION INFORMATION

Serial Interface Description

The A1332 features an I²C compliant interface for communication with a host microcontroller, or Master. A basic circuit for configuring the A1332 package is shown in Figure 4. It is recommended that both the SCL and SDA lines be tied to 3.3 V via a 1 k Ω pull-up resistor. If using a Pull-Up voltage of 5 V, it is recommended to limit current by using a higher value pull-up resistance than 1 K.

If the SDA pin is tied to 5 V, instead of 3.3 V, this results in the forward biasing of an internal diode in the A1332 which could conduct current into the digital voltage regulator internal to the device. This may result in degraded voltage regulation performance. Current-limiting resistors have been implemented on-chip to limit this effect. Measurements show that exposure to this condition does not damage the IC in any permanent manner. However, for best results, it is recommended that the Serial Logic pins SDA and SCL be tied to 3.3 V and not 5 V VCC.

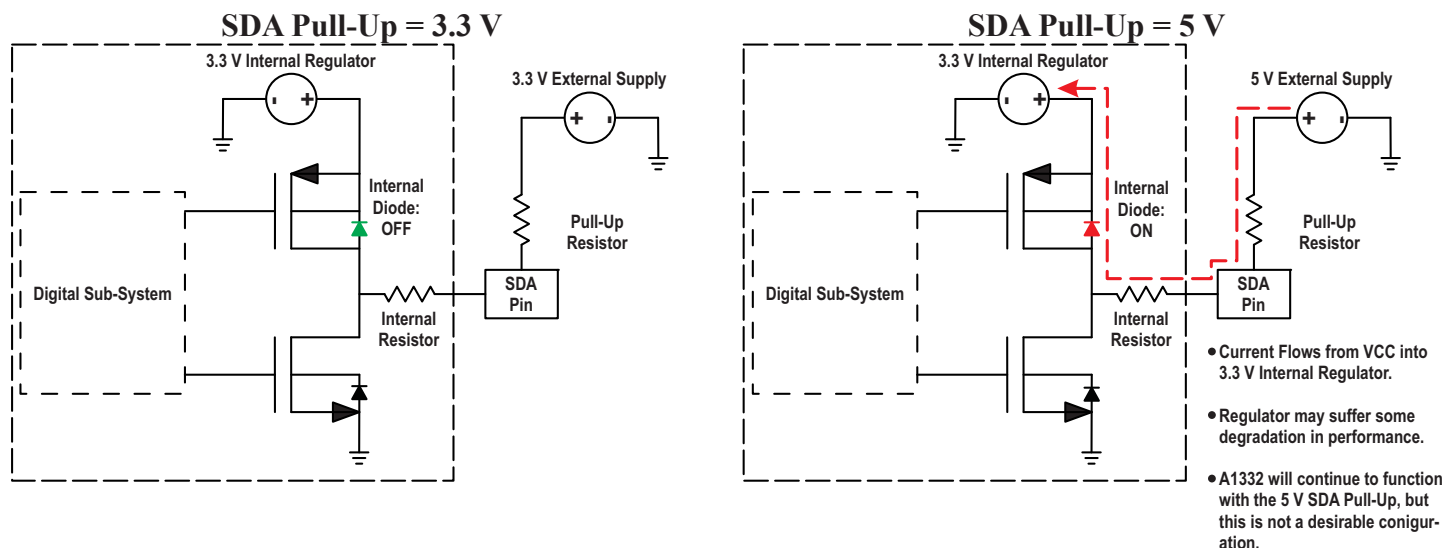


Figure 4: SDA Pin Schematic

Magnetic Target Requirements

There are two main sensing configurations for magnetic angle sensing, on axis and off axis. On-axis (end of shaft) refers to when the center axis of a magnet lines up with the center of the sensing element. Off-axis (side shaft) refers to when the angle sensor is mounted along the edge of a magnet. Figure 9 illustrates on and off axis sensing configurations.

ON-AXIS APPLICATIONS

Some common on-axis applications for the device include digital potentiometer, motor sensing, power steering, and throttle sensing. The A1332 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 1. The device has two internal linearization algorithms that can compensate for much of the error due to alignment. Contact Allegro for more detailed information on magnet selection and theoretical error.

OFF-AXIS APPLICATIONS

There are two major challenges with off axis angle sensing applications. The first is field strength. All efforts should be conducted to maximize magnetic signal strength as seen by the device. The goal is a minimum of 300 G. Field strength can be maximized by using high quality magnetic material, and by minimizing the distance between the sensor and the magnet. Another challenge is overcoming the inherent non-linearity of the magnetic field vector generated at the edge of a magnet. The device has two linearization algorithms that can compensate for much of the geometric error. Harmonic linearization is recommended for off-axis applications.

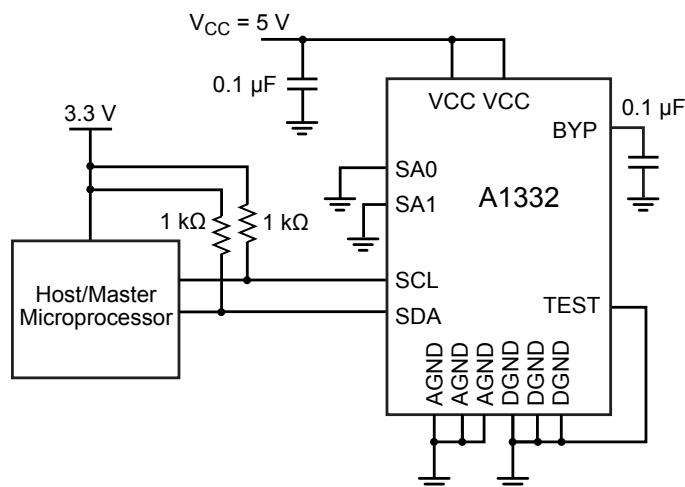
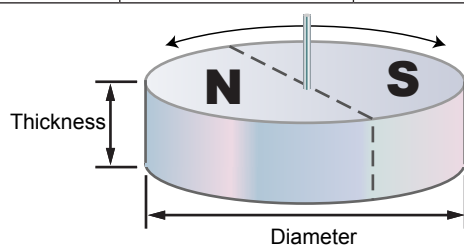


Figure 5: Typical A1332 Configuration
A1332 set up for serial address 0xC

Table 1: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (bonded)	15	4
Neodymium (sintered)*	10	4
Neodymium (sintered)	8	3
Neodymium / SmCo	6	2.5



*A sintered Neodymium magnet with 10 mm (or greater) diameter and 4 mm thickness is the recommended magnet for redundant applications.

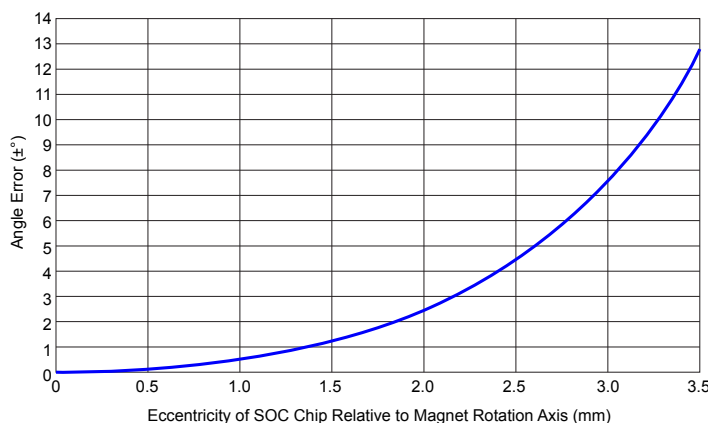
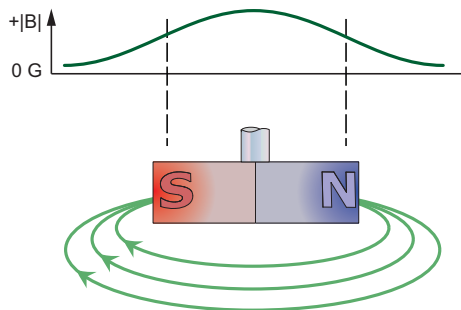


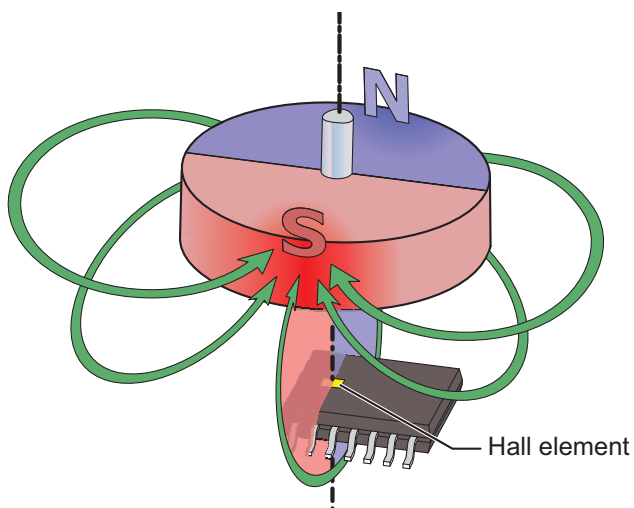
Figure 6: Simulated Error versus Eccentricity for a 10 mm x 4 mm Neodymium Magnet at a 2.7 mm Air Gap.

Typical Systemic Error versus magnet to sensor eccentricity (d_{axial}). Note: "Systemic Error" refers to application errors in alignment and system timing. It does not refer to sensor IC device errors. The data in this graph is simulated with ideal magnetization.

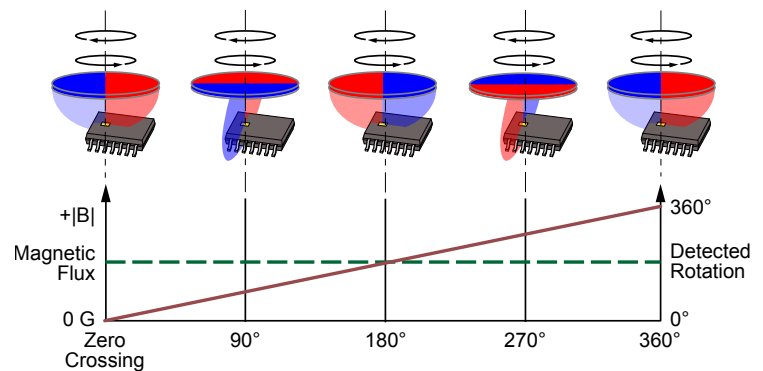
Effect of Orientation on Signal

**Figure 7: Magnetic Field Flux Lines**

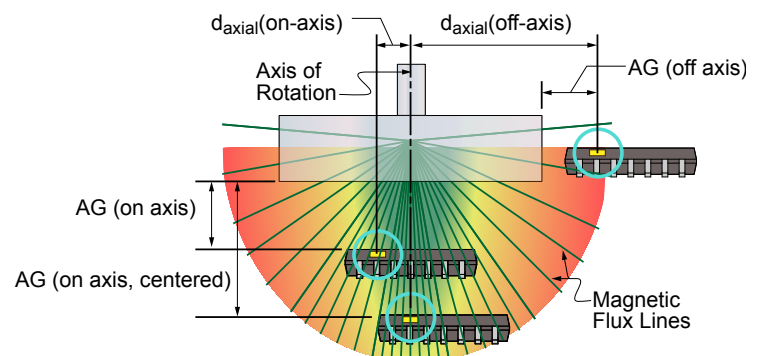
The magnetic field flux lines run fixed field lines coming out of the north pole and going into the south pole of the magnet. The peak flux densities are between the poles.

**Figure 9: Centering the Axis of Magnet Rotation on the Hall Element**

Centering the axis of magnet rotation on the Hall element provides the strongest signal in all degrees of rotation.

**Figure 8: Hall Element Detects Rotating Relative Polarity of Magnetic Field**

As the magnet rotates, the Hall element detects the rotating relative polarity of the magnetic field (solid line); when the center of rotation is centered on the Hall element, the magnetic flux amplitude is constant (dashed line).

**Figure 10: Rapid Degeneration of Magnetic Flux Density**

The magnetic flux density degenerates rapidly away from the plane of peak north-south polarity. When the axis of rotation is placed away from the Hall element, the device must be placed closer to the magnetic poles to maintain an adequate level of flux at the Hall element.

Linearization

Magnetic fields are generally not completely linear throughout the full range of target positions. This can be the result of non-uniformities in mechanical motion or of material composition. In some applications, it may be required to apply a mathematical transfer function to the angle that is reported by the A1332.

The A1332 has built-in functions for performing linearization on the acquired angle data. It is capable of performing one of two different linearization methods: harmonic linearization and piecewise (segmented) linearization.

Segmented linearization breaks up the output dynamic range into 16 equal segments. Each segment is then represented by the equation of a straight line between the two endpoints of the segment. Using this basic principle, it is possible to tailor the output response to compensate for mechanical non-linearity.

One example is a fluid level detector in a vehicle fuel tank. Because of requirements to conform the tank and to provide stiffening, fuel tanks often do not have a uniform shape. A level detector with a linear sensor in this application would not correctly indicate the remaining volume of fuel in the tank without some mathematical conversion. Figure 11 graphically illustrates the general concept.

Harmonic linearization utilizes the Fourier series in order to compensate for periodic error components. In the most basic of terms, the Fourier series is used to represent a periodic signal

using a sum of ideal periodic waveforms. The A1332 is capable of utilizing up to 15 Fourier series components to linearize the output transfer function.

While it can be used for many applications, harmonic linearization is most useful for 360-degree applications. The error curve for a rotating magnet that is not perfectly aligned will most often have an error waveform that is periodic. This phenomenon is especially true for systems where the sensor is mounted off-axis relative to the magnet. Figure 12 illustrates this periodic error.

An initial set of linearization coefficients is created by characterizing the application experimentally. With all signal processing options configured, the device is used to sense the applied magnetic field, B: at a target zero-degrees of rotation reference angle and at regular intervals. For segmented linearization, 16 samples are taken: at nominal zero degrees and every 1/16 interval (22.5°) of the full 360° rotational input range. Each angle is read from the ANG[ANGLE] register and recorded.

These values are loaded into the Allegro ASEK programming utility for the device, or an equivalent customer software program, and to generate coefficients corresponding to the values. The user then uses the software load function to transmit the coefficients to the EEPROM. Each of the coefficient values can be individually overwritten during normal operation by writing directly to the corresponding SRAM.

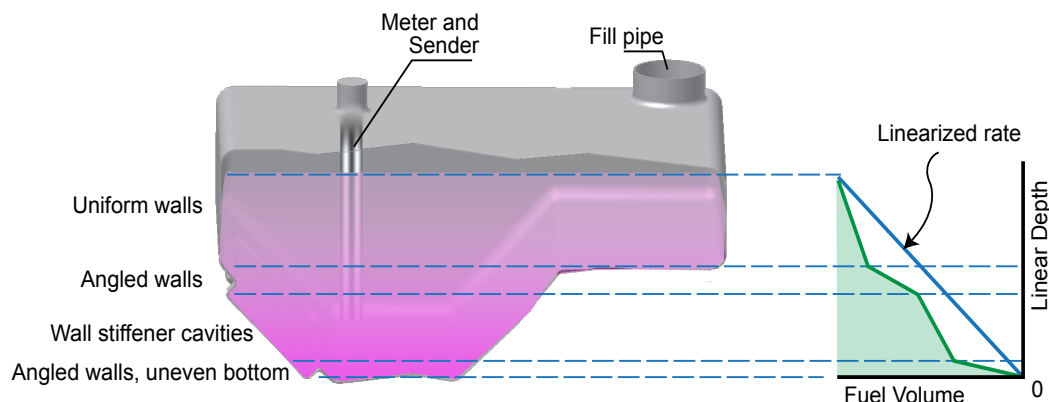


Figure 11: Varying Volumes in an Integrated Vehicle Fuel Tank

An integrated vehicle fuel tank has varying volumes according to depth due to structural elements. As shown in the chart, this results in a variable rate of fuel level change, depending on volume at the given depth, and a linearized transfer function can be used against the integral volume.

Correction for Eccentric Orientation

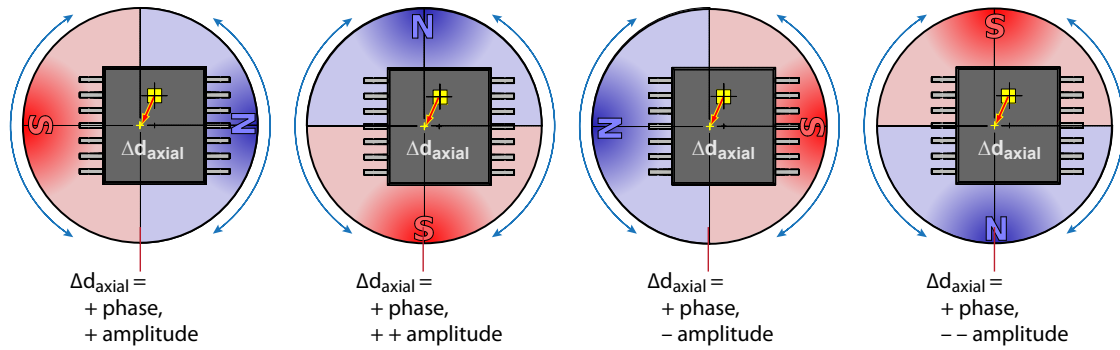


Figure 12a: Linearization Coefficients
With the axis of rotation aligned with the Hall element, linearization coefficients are a simple inversion of the input.

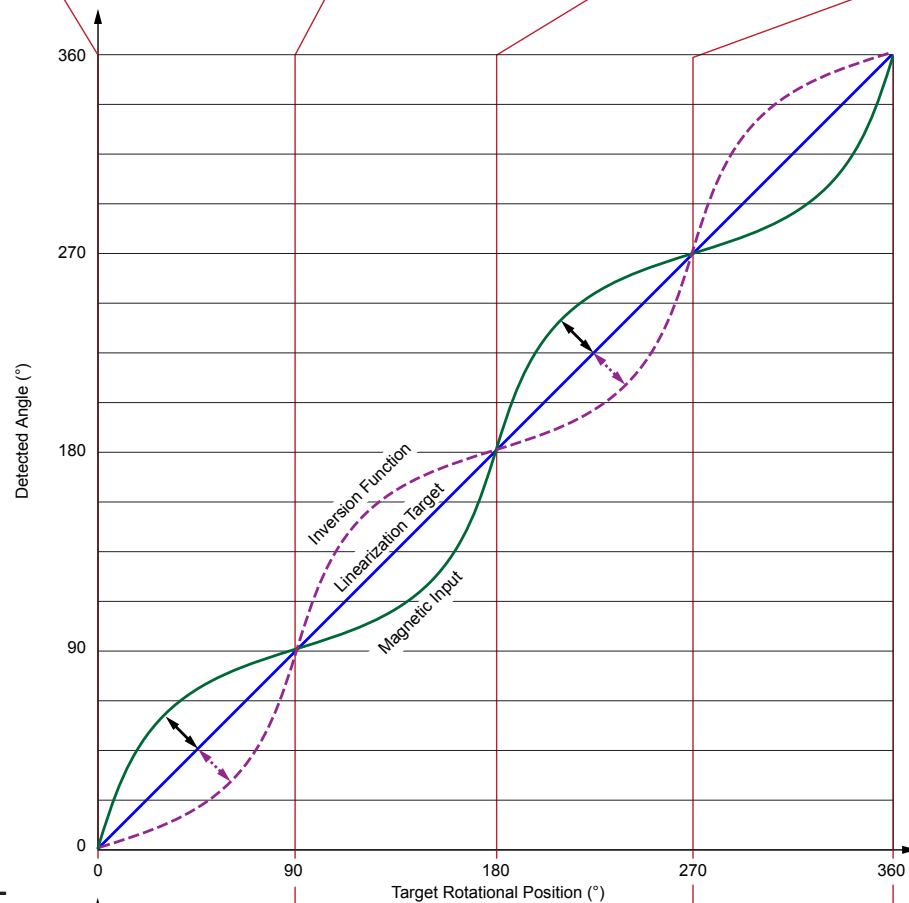
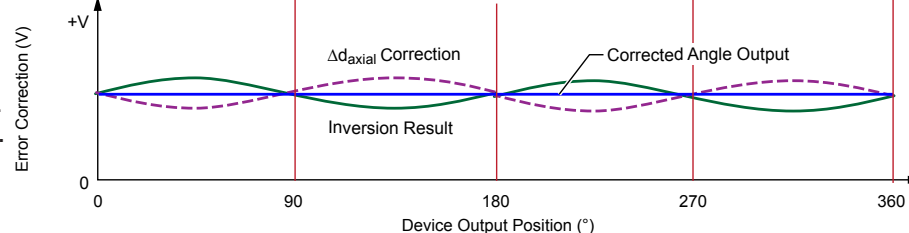


Figure 12b: Any Eccentricity is Evaluated as an Error.

Systematic eccentricity can be factored out by appropriate linearization coefficients. For off-axis applications, the harmonic linearization method is recommended.



HARMONIC COEFFICIENTS

The device supports up to 15 harmonics. Each harmonic is characterized by an amplitude and a phase coefficient.

To apply harmonic linearization, the device:

1. Calculates the error factors.
2. Applies any programmed offsets.
3. Calculates the linearization factor as:

$$A_n \times \sin(n \times t + \varphi_n)$$

PCB Layout

Bypass and decoupling capacitor should be placed as close as possible to corresponding pins, with low impedance traces. Capacitors should be tied to a low impedance ground plane whenever possible.

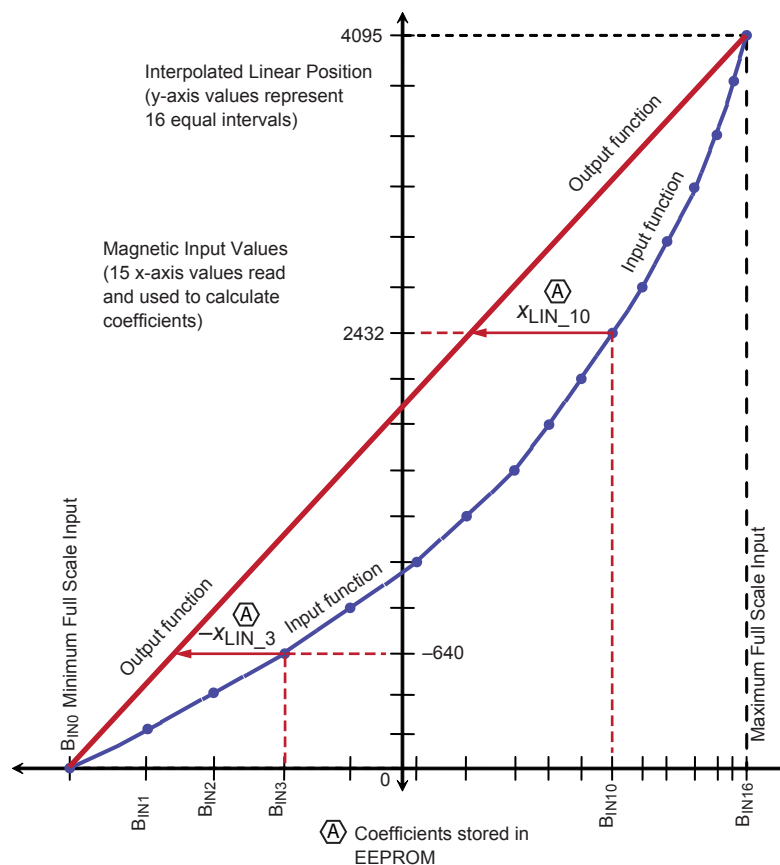


Figure 13: Sample of Linearization Function Transfer Characteristic.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference MO-153 AB-1)

NOT TO SCALE

Dimensions in millimeters

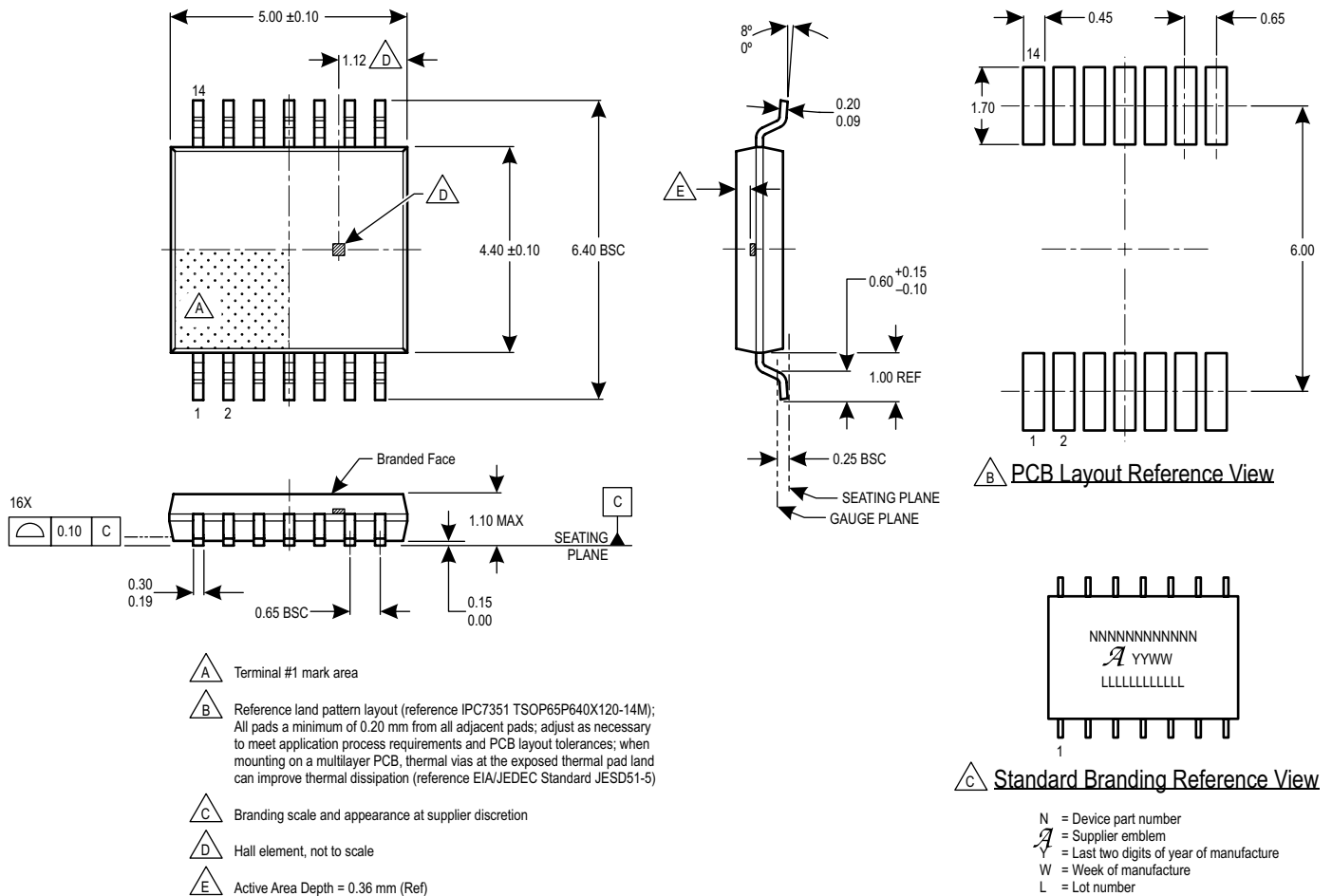
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

Figure 14: Package LE, 14-Pin TSSOP (Single Die Version)

Revision History

Revision No.	Revision Date	Description
–	September 11, 2014	Initial release

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