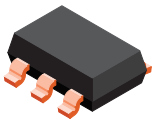
# 2D, Dual-Channel, Ultrasensitive Hall-Effect Latch

## FEATURES AND BENEFITS

- 2D magnetic sensing via planar and vertical Hall elements
- Phase separation between the two channels is inherently 90°
- Dual-channel output allows independent use of Z-axis planar Hall in conjunction with vertical Hall:
  - □ Y-axis (A1262LLH-T)
  - □ X-axis (A1262LLH-X-T)
- High sensitivity, $B_{OP}$ typically 17 G
- Automotive grade
  - □ AEC-Q100 qualified for use in automotive applications
  - □ Output short-circuit protection
  - □ Resistant to physical stress
  - □ Reverse-battery protection
  - □ Solid-state reliability
  - □ Superior temperature stability
  - □ Supply voltage Zener clamp
- Small size

## PACKAGE:

**5-Pin SOT23-W (Suffix LH)**



*Not to scale*

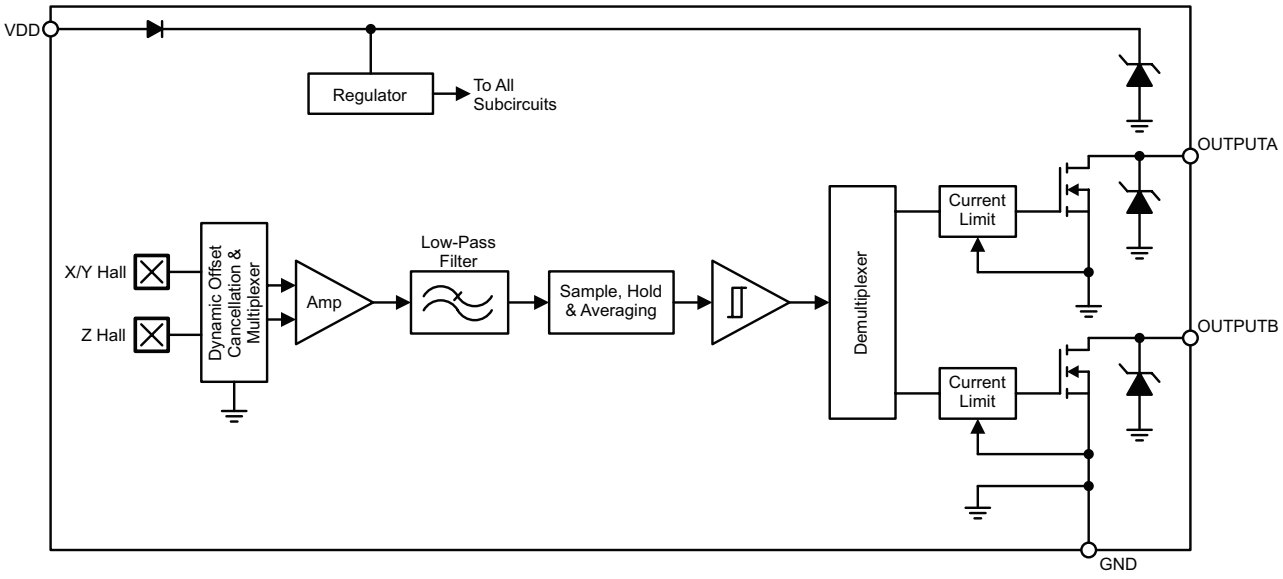
## DESCRIPTION

The A1262 integrated circuit is an ultrasensitive Hall-effect latch. It features operation with traditional planar magnetic field direction as well as vertical. The dual operation of the planar and vertical Hall elements allows the end user to achieve 90° of phase separation that is inherently independent of magnetic pole spacing. The quadrature outputs of the A1262 allow rotation direction to be determined, such as when sensing a rotating ring-magnet target.

The A1262 is available in two options that allow flexibility in end-system magnetic design. Both options feature a planar Hall plate that is sensitive to magnetic fields perpendicular to the face of the package (Z). The primary option features a vertical Hall plate that is sensitive to magnetic fields parallel with the face of the package across the leaded edges of the package (Y). The -X option features a vertical Hall plate that is sensitive to magnetic fields parallel with the face of the package across the leadless edges of the package (X), resulting in lower total effective air gap.

On a single silicon chip, the device includes: two Hall plates (one planar and one vertical), a multiplexer, a small-signal amplifier, chopper stabilization, a Schmitt trigger, and two short-circuit protected NMOS output transistors to sink up

*Continued on the next page…*




**Functional Block Diagram**

## Description (continued)

to 20 mA. The A1262 features circuitry that provides automotive ruggedness and allows operation from 4 to 24 V over a temperature range of –40°C to 150°C.

The small geometries of the BiCMOS process allow these devices to be offered in an ultrasmall package suitable for most applications.

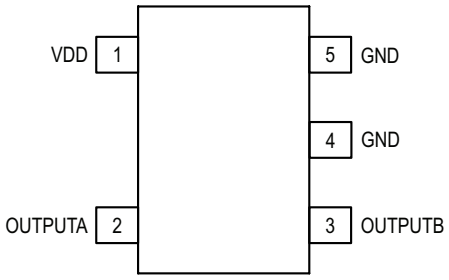
Package designator "LH5" is a modified SOT23-W surface-mount package, magnetically optimized for a variety of orientations. This package is lead (Pb) free, with 100% matte-tin leadframe plating.

## SPECIFICATIONS

### Selection Guide

| Part Number | Packing | Package | Description |
|---|---|---|---|
| A1262LLHLT-T | 7-in. reel, 3000 pieces/reel | LH5 | 2 Outputs of Y and Z |
| A1262LLHLX-T | 13-in. reel, 10000 pieces/reel | LH5 | 2 Outputs of Y and Z |
| A1262LLHLT-X-T* | 7-in. reel, 3000 pieces/reel | LH5 | 2 Outputs of X and Z |
| A1262LLHLX-X-T* | 13-in. reel, 10000 pieces/reel | LH5 | 2 Outputs of X and Z |

* Contact Allegro regarding availability.




**Package LH, 5-Pin SOT23W Pin-Outs**

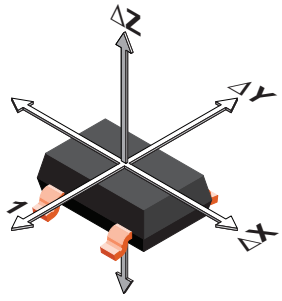



**Table 4: Terminal List Table**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Connects power supply to chip |
| 2 | OUTPUTA | Output of Z magnetic field direction[1] |
| 3 | OUTPUTB | A1262LLH-T: Output of Y magnetic field direction |
| | | A1262LLH-X-T: Output of X magnetic field direction |
| 4 | GND | Ground |
| 5 | GND | Ground |

[1] Z-axis recommended for use as the speed channel in a speed and direction application, due to better repeatability.

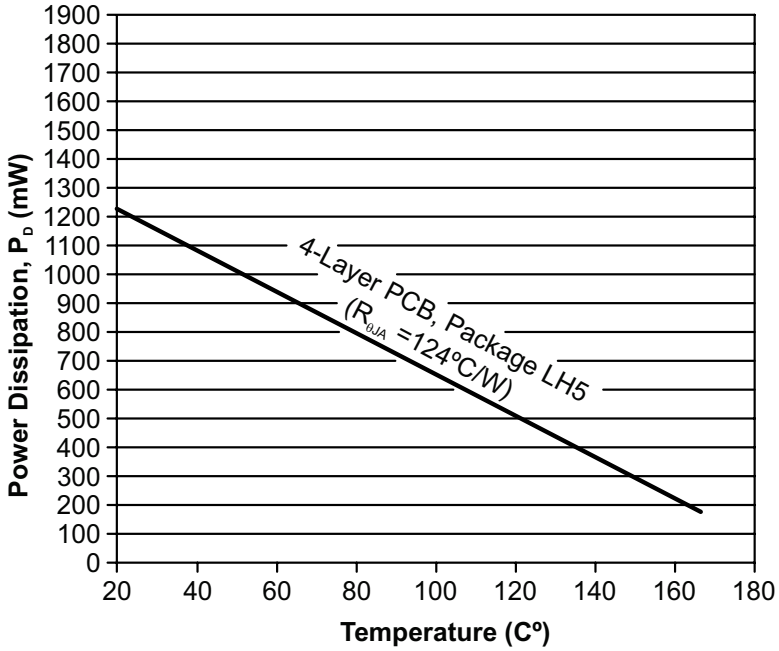
### Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Forward Supply Voltage | $V_{DD}$ | | 26.5 | V |
| Reverse Supply Voltage | $V_{RDD}$ | | –16 | V |
| Magnetic Flux Density | B | | Unlimited | G |
| Output Off Voltage | $V_{OUT}$ | | 26.5 | V |
| Output Sink Current | $I_{OUT(Sink)}$ | | Internally Limited | mA |
| Operating Ambient Temperature | $T_A$ | Range L | –40 to 150 | °C |
| Maximum Junction Temperature[2] | $T_{J(MAX)}$ | | 165 | °C |
| Storage Temperature | $T_{stg}$ | | –65 to 170 | °C |

### THERMAL CHARACTERISTICS may require derating at maximum conditions; see application information

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| Package Thermal Resistance | $R_{\theta JA}$ | Package LH5 4-layer board based on the JEDEC standard | 124 | °C/W |

* Additional thermal information available on the Allegro website.




**Maximum Power Dissipation versus Ambient Temperature**

**ELECTRICAL CHARACTERISTICS:** **Valid over full operating voltage and ambient temperature ranges, unless otherwise specified.**

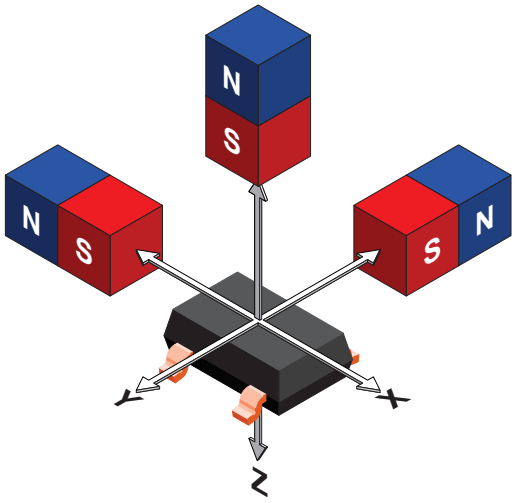
| Characteristics | Symbol | Test Conditions | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | Operating, $T_J$ < 165°C | 4 | – | 24 | V |
| Output Leakage Current | $I_{OUTOFF}$ | B < $B_{RP}$ | – | – | 10 | µA |
| Output On Voltage | $V_{OUT(SAT)}$ | $I_{OUT}$ = 20 mA, B > $B_{OP}$ | – | 180 | 500 | mV |
| Supply Current | $I_{DD}$ | | – | 3 | 7.5 | mA |
| Reverse-Battery Current | $I_{RDD}$ | $V_{RDD}$ = –16 V | – | – | –5 | mA |
| Supply Zener Clamp Voltage | $V_Z$ | $I_{CC}$ = 5 mA; $T_A$ = 25°C | 28 | 34 | – | V |
| Output Sink Current | $I_{OUTPUT(SINK)}$ | | – | – | 20 | mA |
| Output Sink Current, Continuous | $I_{OUTPUT(SINK)C}$ | $T_J$ < $T_{J(max)}$, $V_{OUT}$ = 12 V | 30 | – | 60 | mA |
| Output Sink Current, Peak | $I_{OUTPUT(SINK)P}$ | t < 3 seconds | – | – | 110 | mA |
| Chopping Frequency | $f_C$ | | – | 800 | – | kHz |
| Output Rise Time [2,3] | $t_r$ | $R_L$ = 820 Ω, $C_S$ = 20 pF | – | 0.2 | – | µs |
| Output Fall Time [2,3] | $t_f$ | $R_L$ = 820 Ω, $C_S$ = 20 pF | – | 0.1 | – | µs |
| Power-On Time [2] | $t_{ON}$ | Both channels | – | 32 | 48 | µs |
| Power-On State | POS | | Low | | | |

[1] Typical data are at $T_A$ = 25°C and $V_{DD}$ = 4 V, and are for initial design estimations only.
[2] Power-on time, rise time, and fall time are guaranteed through device characterization.
[3] $C_S$ = oscilloscope probe capacitance.

**MAGNETIC CHARACTERISTICS:** **Valid over full operating voltage and temperature ranges, unless otherwise specified.**

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit [4] |
|---|---|---|---|---|---|---|
| Operate Point [5] | $B_{OP}$ | | 1 | 17 | 40 | G |
| Release Point [5] | $B_{RP}$ | | –40 | –17 | –1 | G |
| Hysteresis | $B_{HYS}$ | $B_{OP}$ – $B_{RP}$ | 15 | 34 | 68 | G |

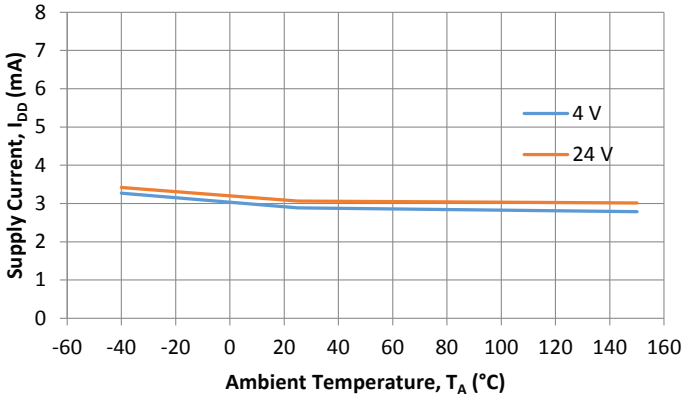
[4] 1 G (gauss) = 0.1 mT (millitesla)
[5] Applicable to all directions (X/Y and Z).



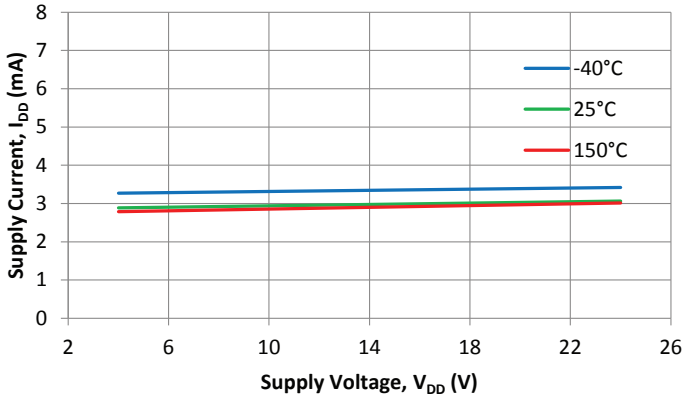

**The A1262 output is turned on when presented with a south polarity magnetic field beyond $B_{OP}$ in the orientations illustrated above. The X-axis field response is only applicable to the A1262LLH-X-T option; the Y-axis field response is only applicable to the A1262LLH-T.**

## CHARACTERISTIC DATA

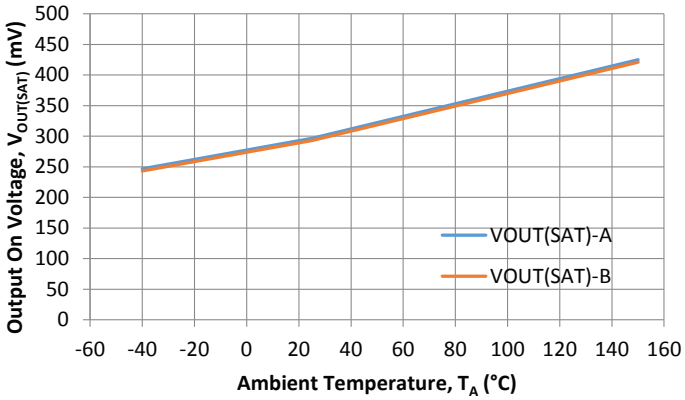
### Average Supply Current vs. Ambient Temperature



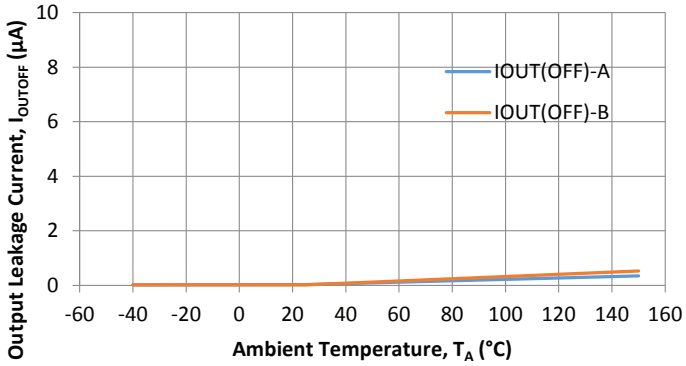

### Average Supply Current vs. Supply Voltage



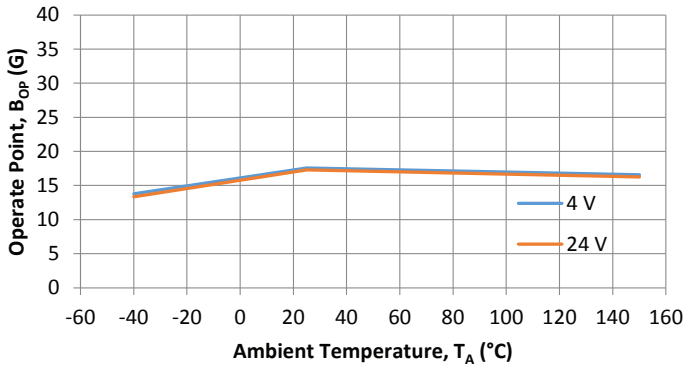

### Avg. Output On Voltage vs. Ambient Temperature



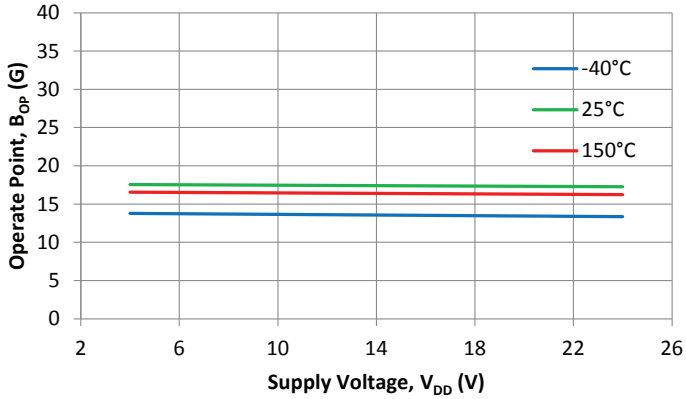

### Avg. Output Leakage Current vs. Ambient Temperature




### Avg. OUTPUTA Operate Point vs. Ambient Temperature

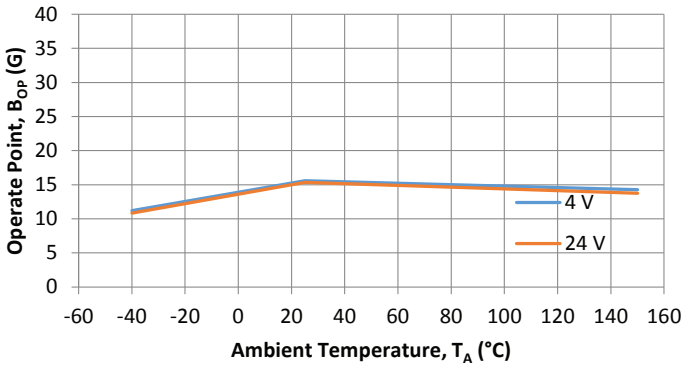



### Avg. OUTPUTA Operate Point vs. Supply Voltage

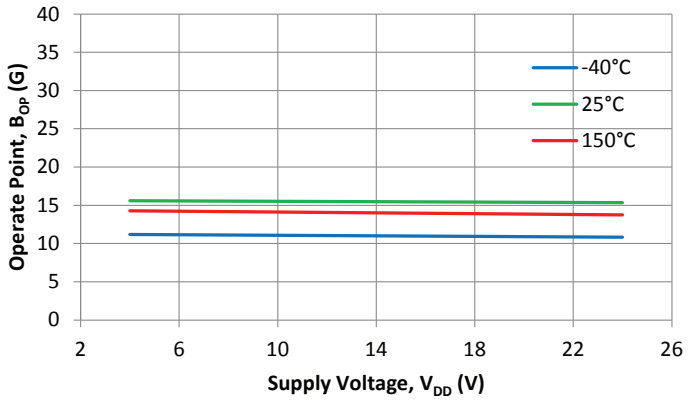


## CHARACTERISTIC DATA (continued)

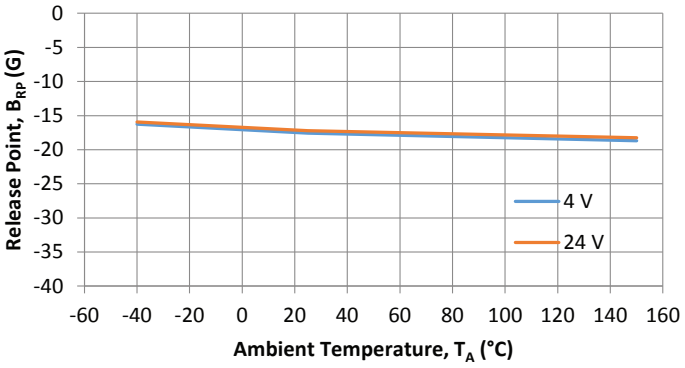
**Avg. OUTPUTB Operate Point vs. Ambient Temperature**



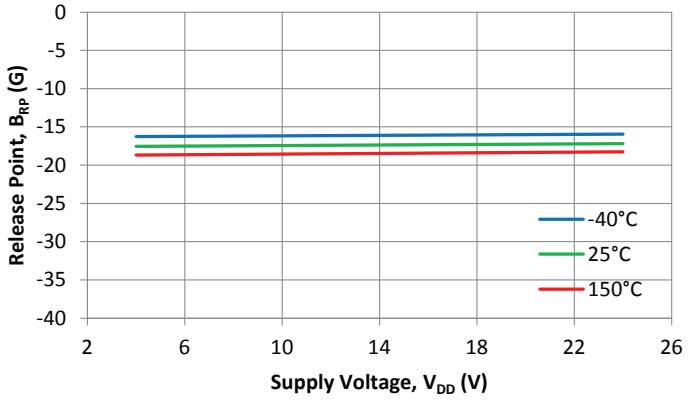

**Avg. OUTPUTB Operate Point vs. Supply Voltage**



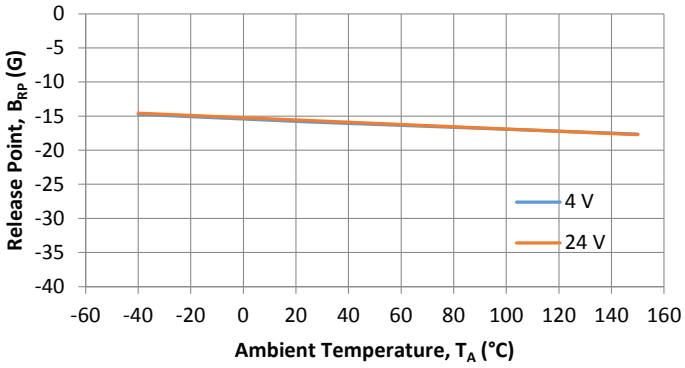

**Avg. OUTPUTA Release Point vs. Ambient Temperature**



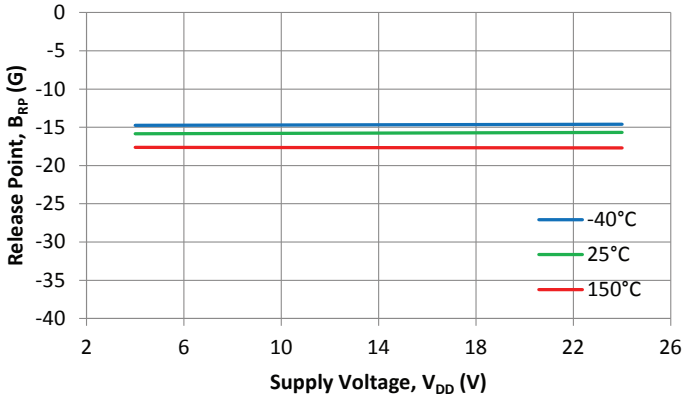

**Avg. OUTPUTA Release Point vs. Supply Voltage**




**Avg. OUTPUTB Release Point vs. Ambient Temperature**

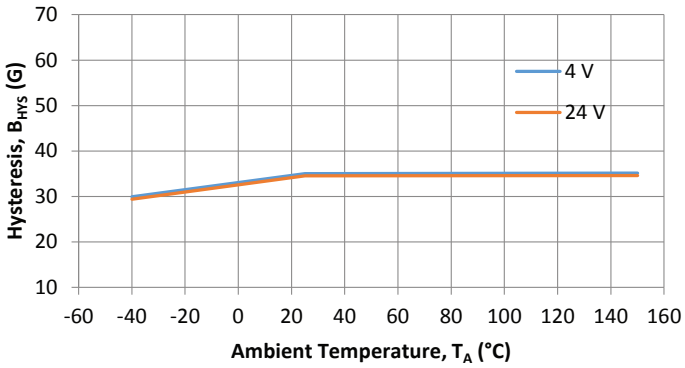



**Avg. OUTPUTB Release Point vs. Supply Voltage**

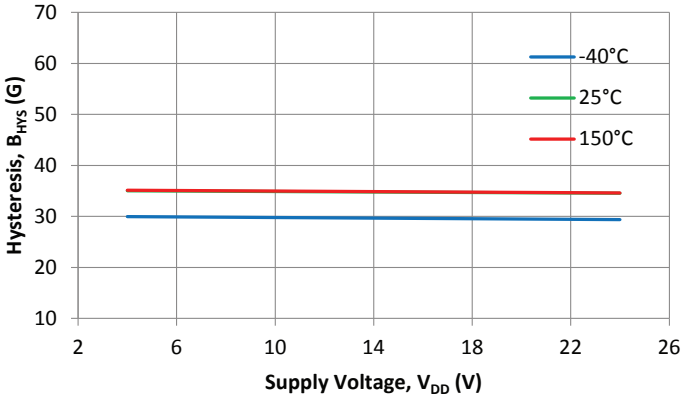


## CHARACTERISTIC DATA (continued)

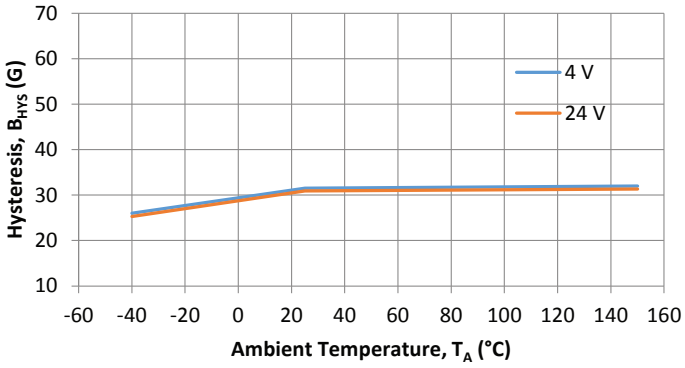
**Avg. OUTPUTA Hysteresis vs. Ambient Temperature**



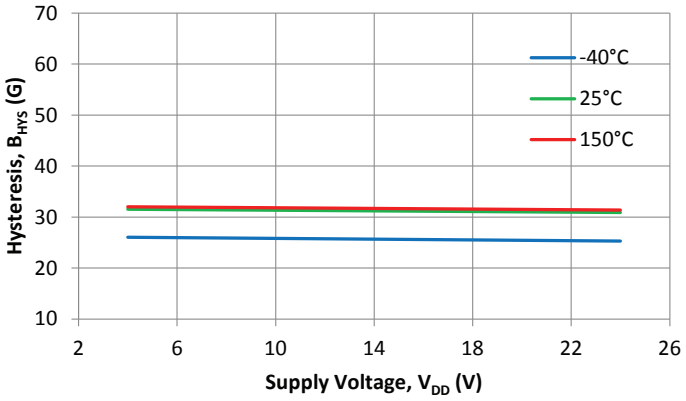

**Avg. OUTPUTA Hysteresis vs. Supply Voltage**



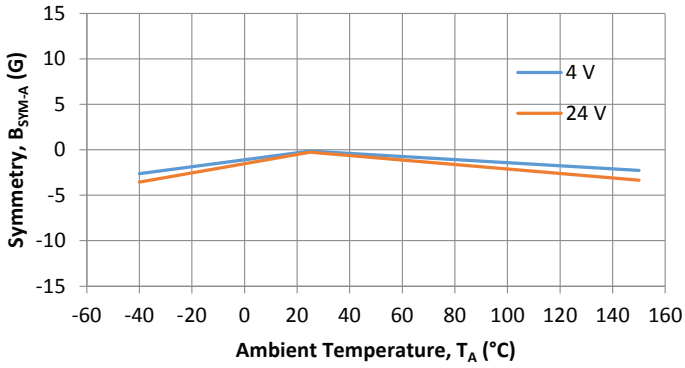

**Avg. OUTPUTB Hysteresis vs. Ambient Temperature**



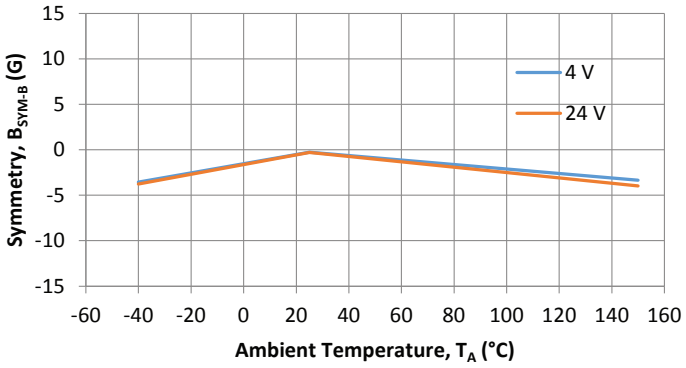

**Avg. OUTPUTB Hysteresis vs. Supply Voltage**




**Avg. $B_{OP-A}$ - $B_{RP-A}$ Symmetry vs. Ambient Temperature**

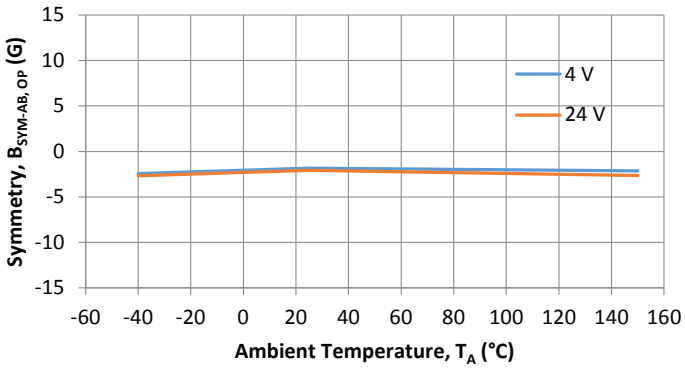



**Avg. $B_{OP-B}$ - $B_{RP-B}$ Symmetry vs. Ambient Temperature**

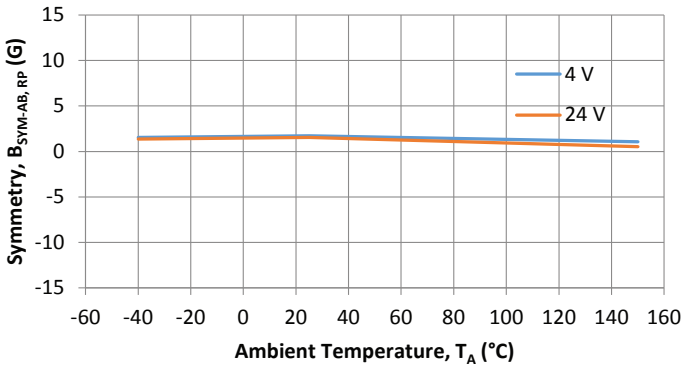


## CHARACTERISTIC DATA (continued)

**Avg. $B_{OP-A}$ - $B_{OP-B}$ Symmetry vs. Ambient Temperature**




**Avg. $B_{RP-A}$ - $B_{RP-B}$ Symmetry vs. Ambient Temperature**



## FUNCTIONAL DESCRIPTION

### Operation

The outputs of the A1262 switch low (turn on) when the corresponding Hall element is presented with a perpendicular south magnetic field of sufficient strength. OUTPUTA switches low if the Z-axis direction exceeds the operate point ($B_{OP}$), and OUTPUTB switches low if the Y-axis direction (A1262LLH-T) or X-axis direction (A1262LLH-X-T) exceeds $B_{OP}$. After turn-on, the output voltage is $V_{OUT(SAT)}$. The device outputs switch high (turn off) when the strength of a perpendicular north magnetic field exceeds the release point ($B_{RP}$). The difference in the magnetic operate and release points is the hysteresis ($B_{HYS}$) of the device. See Figure 1.

Removal of the magnetic field will leave the device output latched on if the last crossed switchpoint is $B_{OP}$, or latched off if the last crossed switchpoint is $B_{RP}$.

This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The device will power-on in the low output state, even when powering-on in the hysteresis region, between $B_{OP}$ and $B_{RP}$.

Unlike dual-planar Hall-effect sensors, which have two planar Hall-effect sensing elements spaced apart across the width of the package, both the vertical and planar sensing elements on the A1262 are located in essentially the same location on the IC.

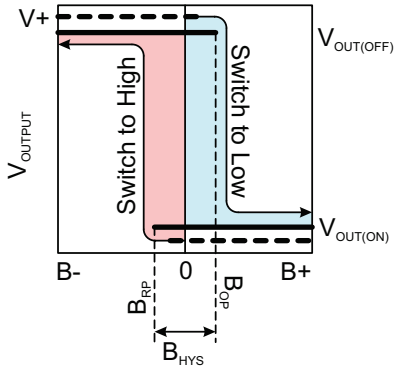



**Figure 1: Switching Behavior of Latches**

**On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity**

With dual-planar Hall sensors, the ring magnet must be properly designed and optimized for the physical Hall spacing (distance) in order to have the outputs of the two latches to be in quadrature, or 90 degrees out of phase. With the A1262, which uses one planar and one vertical Hall-effect sensing element, no target optimization is required. When the face of the IC is facing the ring magnet, the planar Hall senses the magnet poles and the vertical Hall senses the transition between poles, therefore the

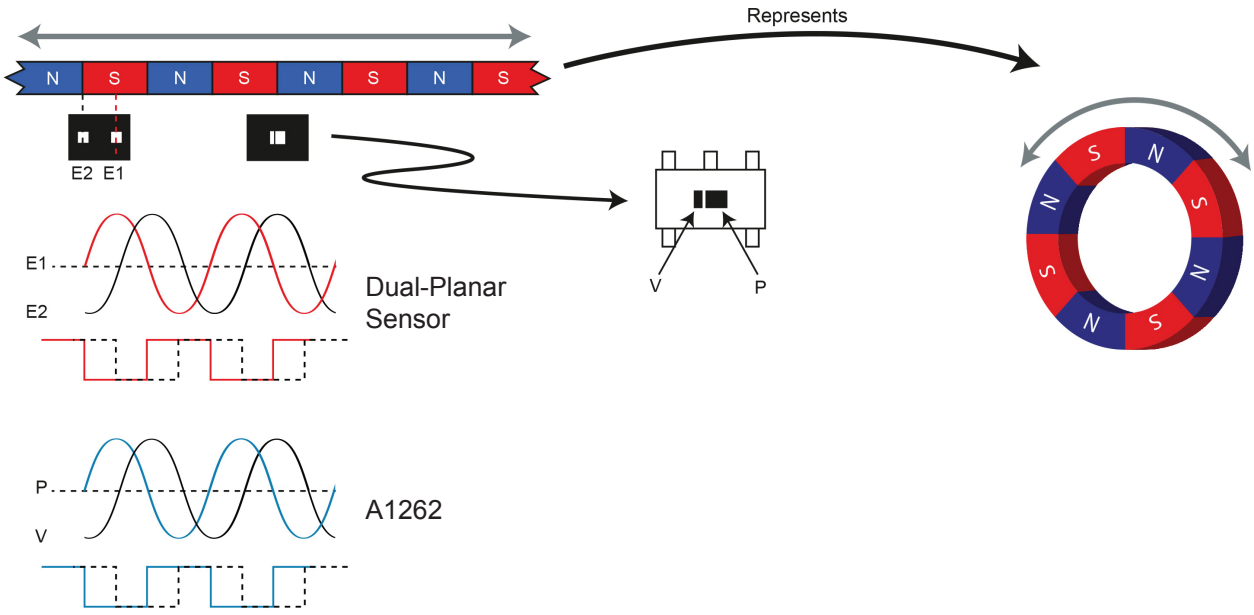



**Figure 2: Ring magnet optimized for a dual-planar Hall-effect sensor resulting in output quadrature also results in quadrature for the A1262.**

two channels will inherently be in quadrature, irrespective of the ring-magnet pole spacing.

Figure 2 above shows a ring magnet optimized for the E1-to-E2 spacing of a dual-planar sensor, resulting in quadrature, or 90 degrees phase separation between channels. This same target also results in quadrature for the 2D sensing A1262. However when a different ring magnet is used which is not optimized for the E1-to-E2 spacing, the dual-planar sensor exhibits diminished phase separation, making signal processing the outputs into speed and direction less robust. Using a different ring-magnet geometry has no effect on the A1262, and the two channels remain in quadrature (see Figure 3 below).

The relationship of the various signals and the typical system timing is shown in Figure 4.

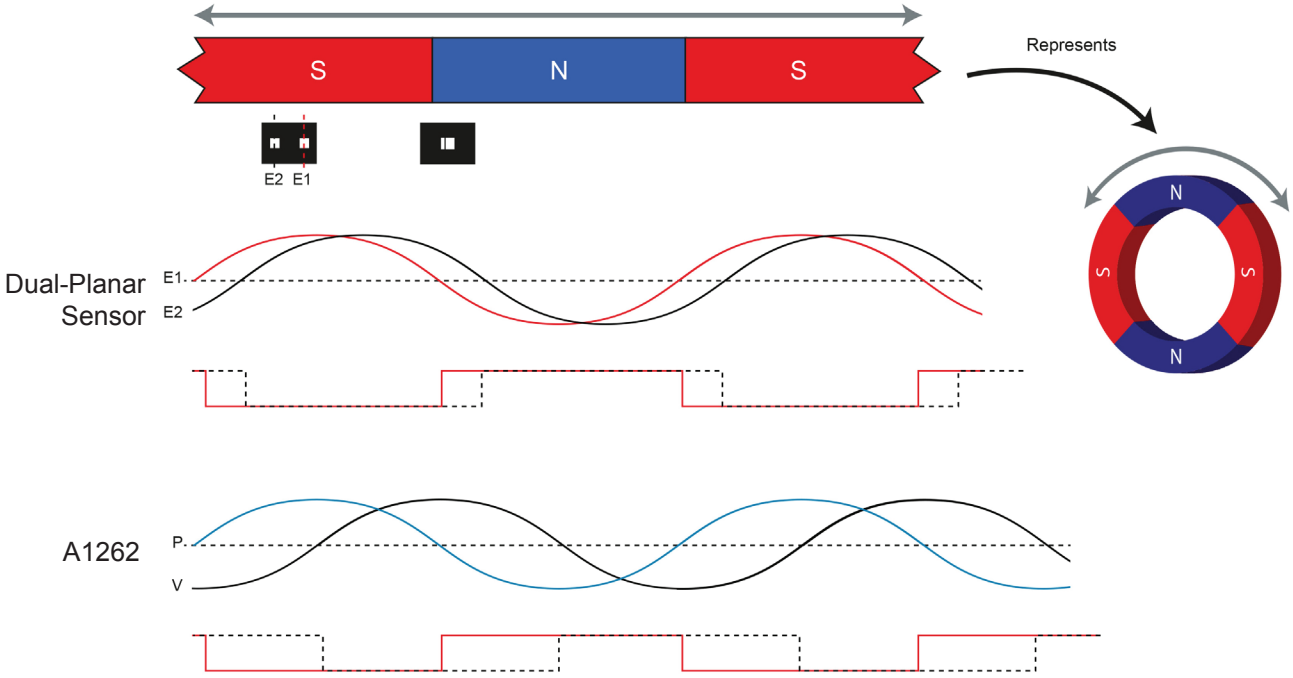



**Figure 3: Ring magnet not optimized for a dual-planar Hall-effect sensor resulting in significantly reduced output phase separation, however still results in quadrature for the A1262.**

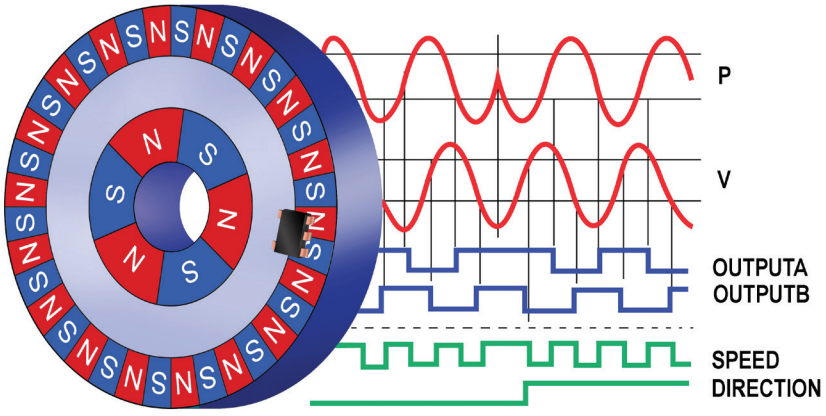



**Figure 4: Typical System Timing**

**The Planar (P) and Vertical (V) signals represent the magnetic input signal, which is converted to the device outputs, OUTPUTA and OUTPUTB, respectively. While the A1262 does not process the signals into Speed and Direction, these could be determined by the user based on the individual output signals.**

## A1262 Sensor and Relationship to Target

The A1262 is available in two options: with Z-axis planar Hall and the Y-axis vertical Hall active, or with the Z-axis planar Hall and the X-axis vertical Hall active. This offers incredible flexibility for positioning the IC within various applications.

The Z-Y option supports the traditional configuration with the face of the package facing the ring magnet (Figure 5a), with the axis of rotation going cross the leads, or with the either of the leaded sides of the package facing the ring magnet (Figure 5b).

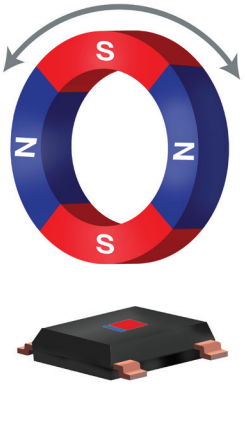



**Figure 5a**

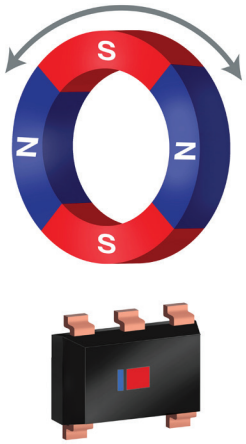



**Figure 5b**

The Z-X option supports having the IC positioned with the face of the package facing the ring magnet, and the axis of rotation (Figure 6a) lengthwise along the package body, or with either of the non-leaded sides of the package facing the ring magnet (Figure 6b). This latter configuration has the advantage of being able to be mounted extremely close to the ring magnet, since there are no leads or solder pads to accommodate for in that dimension.

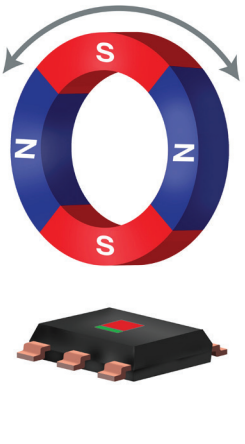



**Figure 6a**

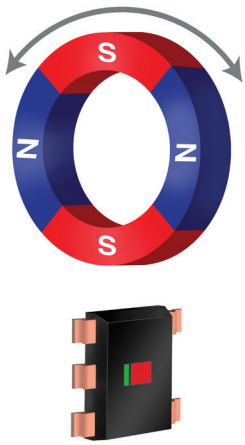



**Figure 6b**

## Power-On Sequence and Timing

The states of OUTPUTA and OUTPUT B are only valid when the supply voltage is within the specified operating range ($V_{DD(MIN)} \le V_{DD} \le V_{DD(MAX)}$) and the power-on time has elapsed ($t > t_{ON}$). Refer to Figure 7: Power-On Sequence and Timing for an illustration of the power-on sequence.

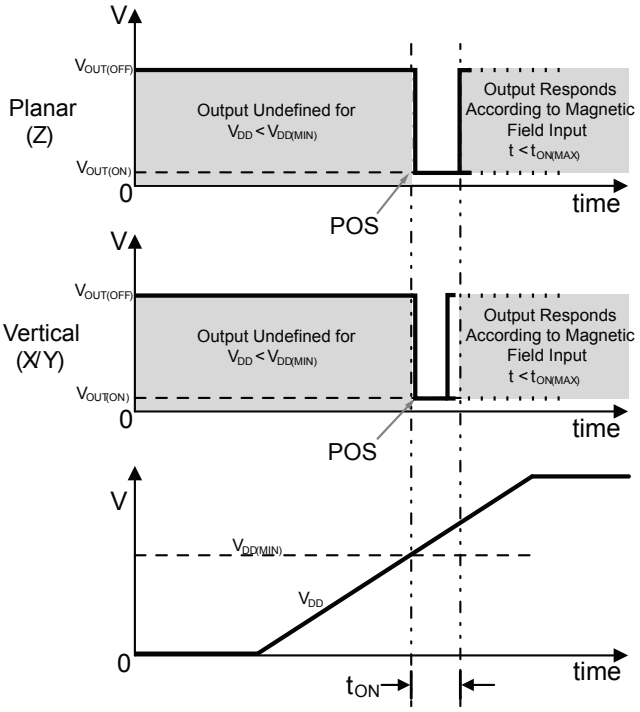



**Figure 7: Power-On Sequence and Timing**

Once the supply voltage is within the operational range, the outputs will be in the low state (power-on state), irrespective of the magnetic field. The outputs will remain low until the sensor is fully powered on ($t > t_{ON}$), at which point, both outputs will respond to the corresponding magnetic field presented to the sensor (the vertical Hall channel typically response before the planar Hall channel).

## Applications

It is strongly recommended that an external capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As shown in Figure 8, a 0.1 µF capacitor is typical.

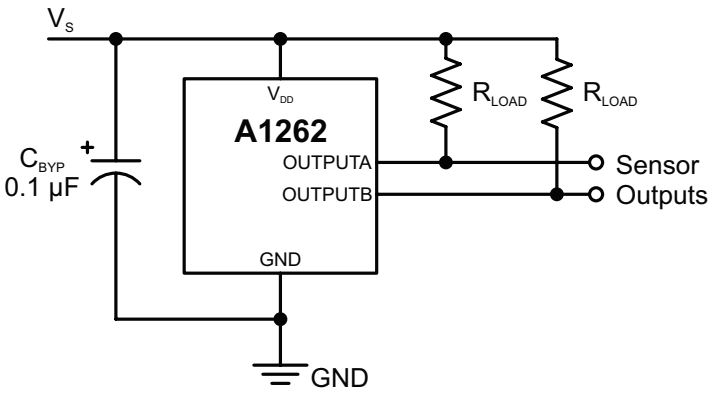



**Figure 8: Typical Application Circuit**

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines for Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMD and Through-Hole, AN26009*

All are provided on the Allegro website:

**www.allegromicro.com**

## Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switch-point accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a proven approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of output drift induced by thermal and mechanical stresses. This technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in Figure 3.

The chopper stabilization technique uses a 400 kHz high-frequency clock. For demodulation process, a sample, hold, and averaging technique is used, where the sampling is performed at twice the chopper frequency (800 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic and sample-and-hold circuits.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high-frequency chopping approach minimizes the effect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields—for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital sensor families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

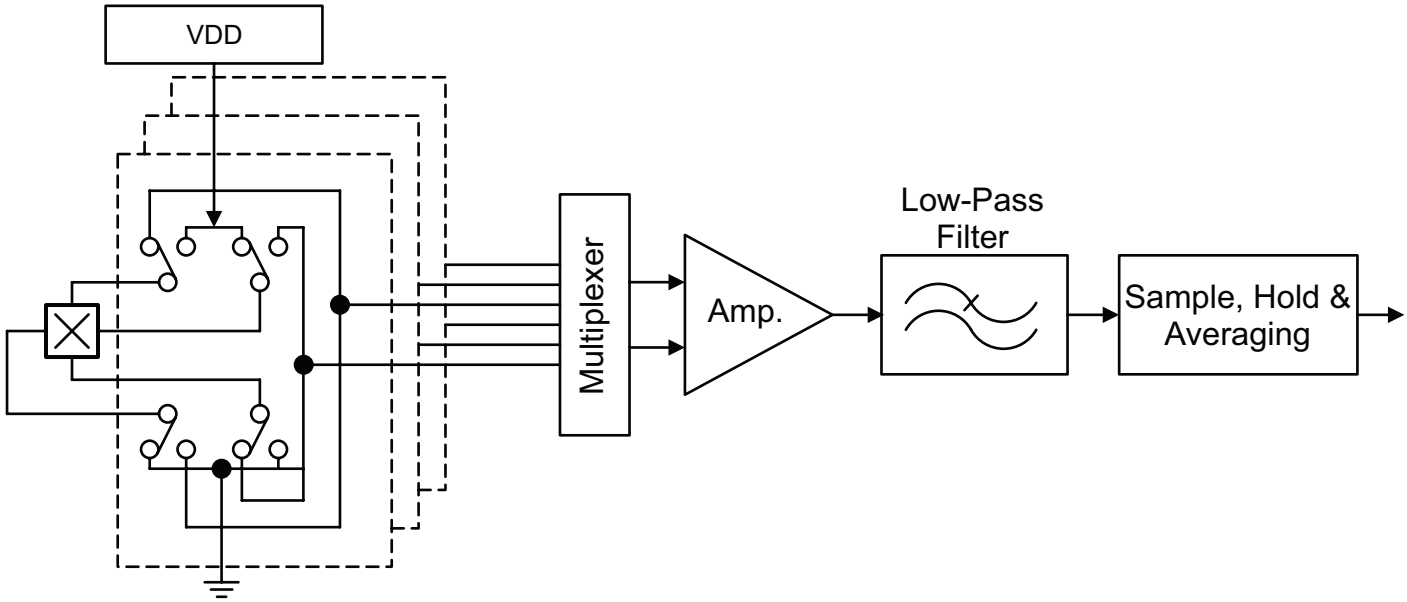



**Figure 3: Model of Chopper Stabilization Technique**

## POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating $T_J$. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature ($T_A$) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, $P_D$), can be estimated. The following formulas represent the fundamental relationships used to estimate $T_J$ at $P_D$.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A$ = 25°C, $V_{DD}$ = 12 V, $I_{DD}$ = 3 mA, and $R_{\theta JA}$ = 124°C/W for the LH5 package, then:

$$P_D = V_{DD} \times I_{DD} = 12\ V \times 3.0\ mA = 36.0\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 36.0\ mW \times 124°C/W = 4.5°C$$

$$T_J = T_A + \Delta T = 25°C + 4.5°C = 29.5°C$$

A worst-case estimate ($P_{D(max)}$) represents the maximum allowable power level ($V_{DD(max)}$, $I_{DD(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and $T_A$.

Example: Reliability for $V_{DD}$ at $T_A$ = 150°C, package LH5, using low-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 124°C/W, $T_{J(max)}$ = 165°C, $V_{DD(max)}$ = 24 V, and $I_{DD(max)}$ = 7.5 mA.

Calculate the maximum allowable power level ($P_{D(max)}$). First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to $T_J$ resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 124°C/W = 121\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{DD(est)} = P_{D(max)} \div I_{DD(max)}$$

$$V_{DD(est)} = 121\ mW \div 7.5\ mA$$

$$V_{DD(est)} = 16.1\ V$$

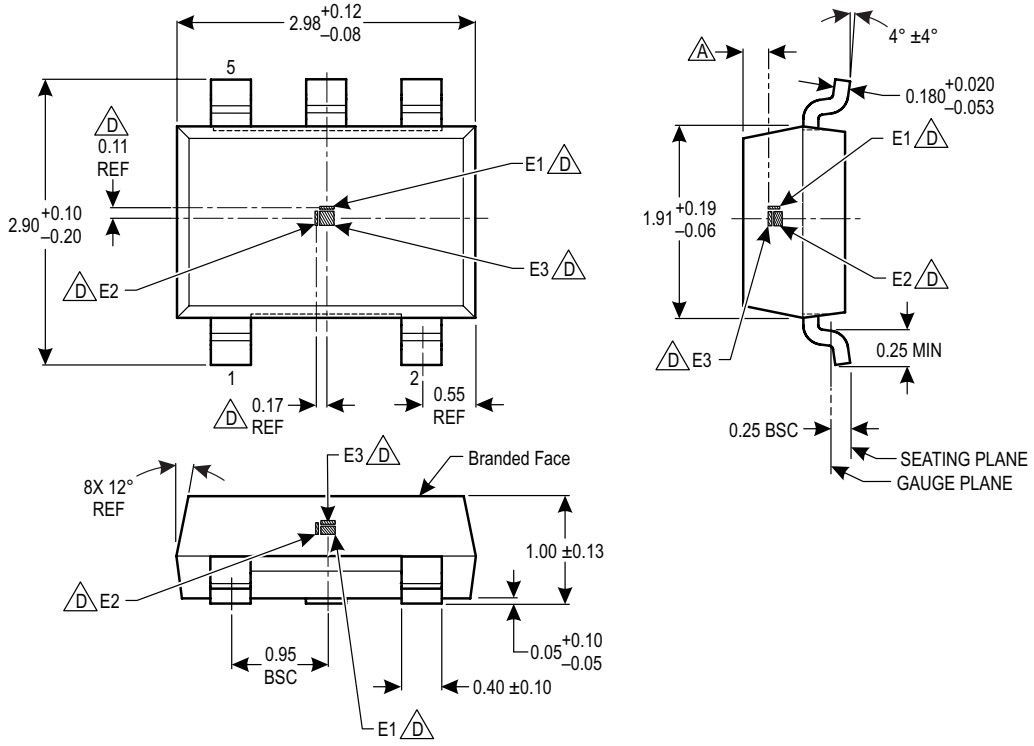
The result indicates that, at $T_A$, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{DD(est)}$.

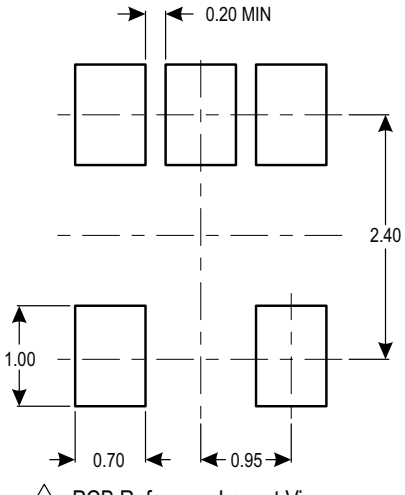
Compare $V_{DD(est)}$ to $V_{DD(max)}$. If $V_{DD(est)} \leq V_{DD(max)}$, then reliable operation between $V_{DD(est)}$ and $V_{DD(max)}$ requires enhanced $R_{\theta JA}$. If $V_{DD(est)} \geq V_{DD(max)}$, then operation between $V_{DD(est)}$ and $V_{DD(max)}$ is reliable under these conditions.

## PACKAGE OUTLINE DRAWING

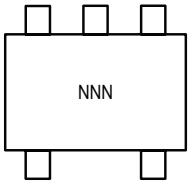
**For Reference Only – Not for Tooling Use**

(Reference DWG-9069)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown




B PCB Reference Layout View




C Standard Branding Reference View

A Active Area Depth, 0.28 ±0.04

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding Scale and appearance at supplier discretion

D Hall Elements (E1, E2, and E3), not to scale; E2 and E3 are active in the A1262LLH-T; E1 and E3 are active in the A1262LLH-X-T

**Figure 4: Package LH, 5-Pin SOT23-W**

## Revision History

| Revision | Revision Date | Description of Revision |
|---|---|---|
| – | September 21, 2015 | Initial Release |



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