88W8987

2.4/5 GHz Dual-band 1x1 Wi-Fi 5 (802.11ac) and Bluetooth 5.0 Solution

Rev. 1 — 8 October 2020 Product short data sheet

1 Product overview

The 88W8987 is a highly integrated Wi-Fi (2.4/5 GHz) and Bluetooth single-chip solution, specifically designed to support the speed, reliability, and quality requirements of next generation Very High Throughput (VHT) products.

The System-on-Chip (SoC) provides both simultaneous and independent operation of the following:

- IEEE 802.11ac (Wave 2), 1x1 with data rates up to MCS9 (433 Mbit/s)
- Bluetooth 5.0 (includes Bluetooth Low Energy (LE))

The SoC also provides:

- Bluetooth Classic and Bluetooth LE dual (Smart Ready) operation
- Wi-Fi indoor location positioning (802.11mc)

For security, the device supports high performance 802.11i security standards through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), AES/Galois/Counter Mode Protocol (GCMP), Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP), AES/Cipher-Based Message Authentication Code (CMAC), and WLAN Authentication and Privacy Infrastructure (WAPI) security mechanisms.

For video, voice, and multimedia applications, 802.11e Quality of Service (QoS) is supported. The device also supports 802.11h Dynamic Frequency Selection (DFS) for detecting radar pulses when operating in the 5 GHz range.

Host interfaces include SDIO 3.0 and high-speed UART interfaces for connecting Wi-Fi and Bluetooth technologies to the host processor.

The device is designed with two front-end configurations to accommodate Wi-Fi and Bluetooth on either separate or shared paths:

- 2-antenna configuration—1x1 Wi-Fi and Bluetooth on separate paths (QFN)
- 1-antenna configuration—1x1 Wi-Fi and Bluetooth on shared paths (eWLP)

The following figures show the application diagrams for each package option.

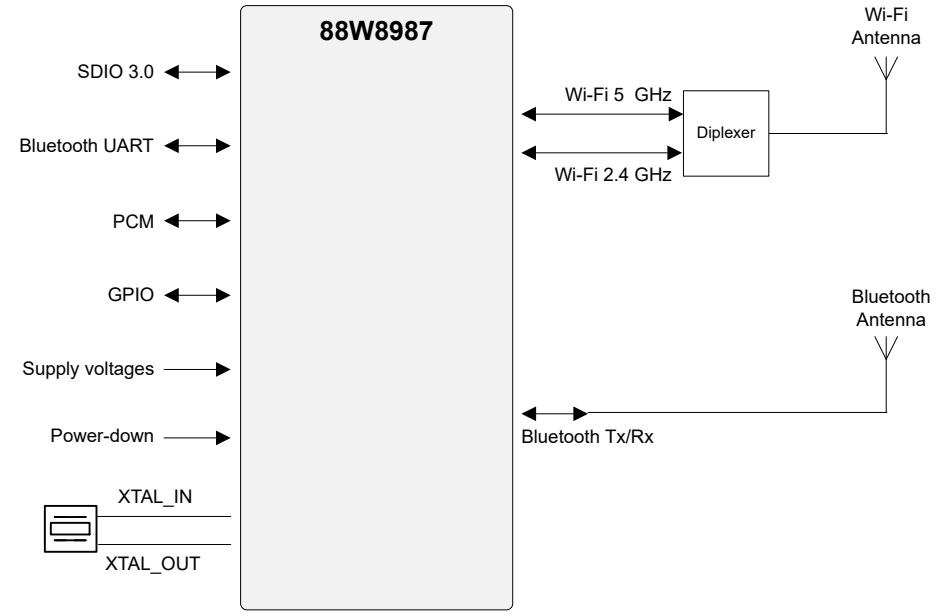


Figure 1. Application diagram—QFN package option

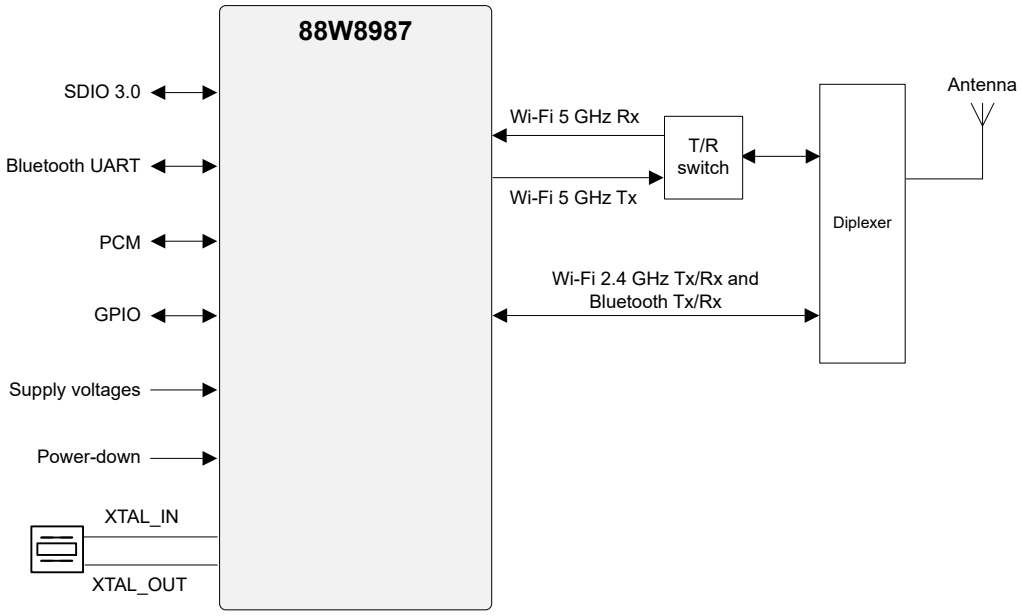


Figure 2. Application diagram—eWLP package option

1.1 Applications

- Wi-Fi and Bluetooth enabled smart phones and tablets
- Personal computing systems including notebooks and ultrabooks
- Wireless home audio and video entertainment systems
- Mobile routers and Internet of Things (IoT) gateways

1.2 Wi-Fi key features

- Support 802.11ac/n/a/g/b
- Dual band: 2.4 GHz and 5 GHz
- Up to MCS9 data rates
- 20/40/80 MHz channel bandwidth
- Security: TKIP, AES, WAPI

1.3 Bluetooth key features

- Bluetooth 5 features
- PCM audio interface
- Security: AES

1.4 Host interfaces

Wi-Fi and Bluetooth host interface options

Wi-Fi	Bluetooth
SDIO 3.0	UART
SDIO 3.0	SDIO 3.0

1.5 Operating characteristics

- Supply voltage: 2.2V, 1.8V, and 1.1V
- Operating temperature
  - Extended: -30 to 85°C
  - Industrial: -40 to 85°C

1.6 General features

- Package options
  - 68-pin 8x8 mm QFN with wettable flanks
  - 83-bump 4.6x4.2 mm eWLP
- Power management
  - Low power dissipation
  - Optional lower power operation with external sleep clock
  - Sleep and standby modes for low-power operation
- Independent ARM-based Wi-Fi and Bluetooth CPUs
- Supports reference clock signal from external crystal or external crystal oscillator
- Memory
  - Internal SRAM
  - Boot ROM
  - One Time Programmable (OTP) memory to store the MAC address and calibration data
- Peripheral interfaces
  - GPIO interface (up to 21)

1.7 Internal block diagram

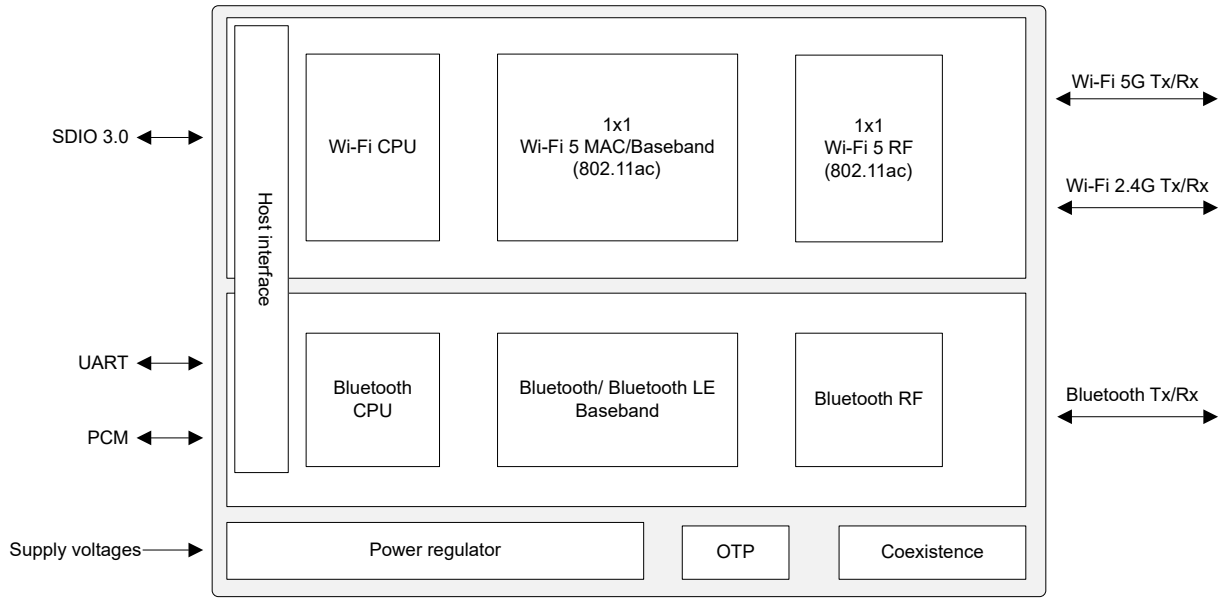


Figure 3. Internal block diagram—QFN package option

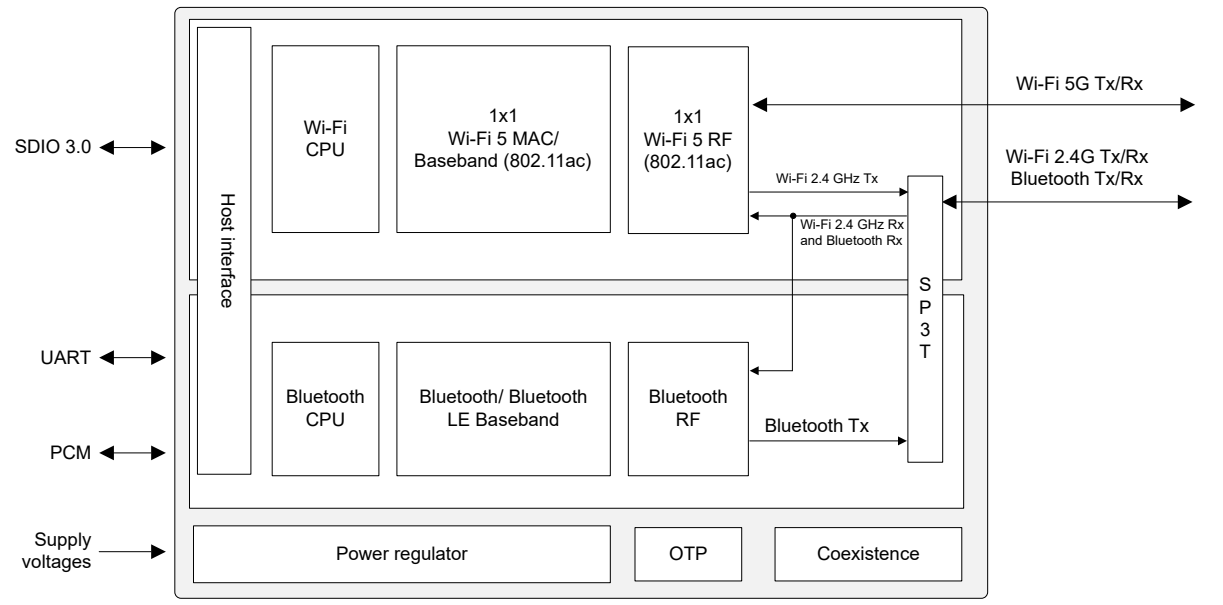


Figure 4. Internal block diagram—eWLP package option

2 Ordering information

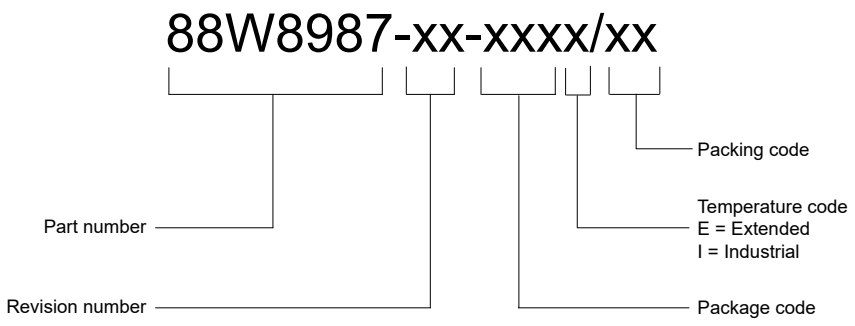


Figure 5. Part numbering scheme

Table 1. Part order codes

Part order code	Package type	Packing
88W8987-A2-NYEE/AK	68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tray
88W8987-A2-NYEE/AZ	68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tape and reel
88W8987-A2-NYEI/AK	68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tray
88W8987-A2-NYEI/AZ	68-pin HVQFN - 8 x 8 x 0.85 mm, with 0.4 mm pitch	Tape and reel
88W8987-A2-EAHE/AZ	83-terminal eWLP - 4.6 x 4.2 x 0.75 mm, with 0.4 mm pitch	Tape and reel

3 Wi-Fi subsystem

3.1 IEEE 802.11 standards

- 802.11 data rates of 1 and 2 Mbit/s
- 802.11b data rates of 5.5 and 11 Mbit/s
- 802.11a/g data rates 6, 9, 12, 18, 24, 36, 48, and 54 Mbit/s for multimedia content transmission
- 802.11g/b performance enhancements
- 802.11ac / 802.11n with maximum data rates up to 86.7 Mbit/s (20 MHz channel), 200 Mbit/s (40 MHz channel), 433 Mbit/s (80 MHz channel)
- 802.11d international roaming
- 802.11e quality of service
- 802.11h transmit power control
- 802.11h DFS radar pulse detection
- 802.11i enhanced security
- 802.11k radio resource measurement
- 802.11mc precise indoor location positioning
- 802.11n block acknowledgment extension
- 802.11r fast hand-off for AP roaming
- 802.11u Hotspot 2.0 (STA mode only)
- 802.11v TIM frame transmission/reception
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode

3.2 Wi-Fi MAC

- Simultaneous peer-to-peer and Infrastructure Modes
- RTS/CTS for operation under DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- On-chip Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation) (supports 802.11ac single-MPDU A-MPDU)
- 20/40/80 MHz coexistence
- Reduced Inter-Frame Spacing (RIFS) receive
- Management information base counters
- Radio resource measurement counters
- Quality of service queues
- Block acknowledgment extension
- Dynamic frequency selection
- Beamforming
  - 802.11ac Explicit Beamformee, supports immediate feedback generation using 802.11ac compressed steering matrix feedback
  - 802.11ac Multi-User Beamformee
  - 802.11n Explicit Beamformee, supports immediate feedback generation using uncompress and compress steering matrix or delayed feedback of all feedback types
- TIM frame transmission/reception
- Multiple-BSS/Station
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Mobile hotspot

3.3 Wi-Fi baseband

- 802.11ac (on-chip RF radio)
- Backward compatibility with legacy 802.11n/a/g/b technology
- Simultaneous Wi-Fi and Bluetooth receive in single-antenna mode (eWLP only)
- PHY data rates up to 433 Mbit/s
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz packets in 40 MHz channel, 20 MHz duplicate legacy packets in 40 MHz channel mode operation
- 80 MHz bandwidth/channel, 4 positions of 20 MHz packets in 80 MHz channel, upper/lower 40 MHz packets in 80 MHz channel, 20 MHz quadruplicate legacy packets in 80 MHz channel mode operation
- Modulation and Coding Scheme (MCS)
  - 802.11ac—MCS 0~9 Nsts = 1
  - 802.11n—MCS 0~7 and MCS 32 (duplicate 6 Mbit/s)
- Dynamic frequency selection (radar detection)
  - Enhanced radar detection for long and short pulse radar
  - Enhanced AGC scheme for DFS channel
  - Japan DFS requirements for W53 and W56 frequency bands
- Radio resource measurement
- Optional 802.11ac and 802.11n features:
  - 20/40/80 MHz coexistence with middle-packet detection (GI detection) for enhanced CCA
  - 1 spatial stream STBC reception
  - LDPC transmission and reception for both 802.11n and 802.11ac
  - 256 QAM (MCS 8, 9) modulation, optional support for 802.11ac MCS 9 in 20 MHz using LDPC
  - Short guard interval
  - RIFS on receive path for 802.11n packets
  - 802.11n greenfield Tx/Rx
  - Explicit beamformee support
  - 802.11ac multi-user beamformee
  - MU-PPDUs (receive)
- Wi-Fi indoor locationing (802.11mc)
- Power save features

3.4 Wi-Fi radio

- Integrated direct-conversion radio
- 20, 40, and 80 MHz channel bandwidths
- Shared Wi-Fi/Bluetooth receive input scheme for 2.4 GHz band (eWLP only)

Wi-Fi Rx path

- Direct conversion architecture eliminates need for external SAW filter
- On-chip gain selectable LNA with optimized noise figure and power consumption
- High dynamic range AGC function in receive mode

Wi-Fi Tx path

- Internal PA with power control
- Optimized Tx gain distribution for linearity and noise performance

Wi-Fi local oscillator

- Fractional-N for multiple reference clock support
- Fine channel step

3.5 Wi-Fi encryption

- Temporal Key Integrity Protocol (TKIP) /
  Wired Equivalent Privacy (WEP)
- Advanced Encryption Standard (AES) / Counter-Mode/CBC-MAC Protocol (CCMP)
- Advanced Encryption Standard (AES) /
  Cipher-Based Message Authentication Code (CMAC)
- Advanced Encryption Standard (AES) / Galois/Counter Mode Protocol (GCMP)
- WLAN Authentication and Privacy Infrastructure (WAPI)

3.6 Wi-Fi host interfaces

- SDIO 3.0 device interface (4-bit SDIO and 1-bit SDIO) transfer modes at full clock range up to 208 MHz

4 Bluetooth subsystem

4.1 2.4 GHz Bluetooth Tx/Rx

- Bluetooth 5
- Bluetooth Class 2
- Bluetooth Class 1
- Single-ended, shared Tx/Rx path for Bluetooth (QFN package option)
- Simultaneous Wi-Fi and Bluetooth receive in single-antenna mode (eWLP package option)
- PCM interface for voice applications
- Baseband and radio BDR and EDR packet types—1 Mbit/s (GFSK), 2 Mbit/s (π/4-DQPSK), and 3 Mbit/s (8DPSK)
- Fully functional Bluetooth baseband—AFH, forward error correction, header error control, access code correlation, CRC, encryption bit stream generation, and whitening
- Adaptive Frequency Hopping (AFH) using Packet Error Rate (PER)
- Interlaced scan for faster connection setup
- Simultaneous active ACL connection support
- Automatic ACL packet type selection
- Full master and slave piconet support
- Scatternet support
- Standard SDIO and UART HCI transport layer
- HCI layer to integrate with profile stack
- SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement
- All standard SCO/eSCO voice coding
- All standard pairing, authentication, link key, and encryption operations
- Standard Bluetooth power saving mechanisms (sniff modes, and sniff sub-rating)
- Enhanced Power Control (EPC)
- Channel Quality Driven Data Rate (CQDDR)
- Wideband Speech (WBS) support (1 WBS link)
- Encryption (AES) support

4.2 Bluetooth Low Energy (LE)

- Broadcaster, Observer, Central, and Peripheral roles
- Supports link layer topology to be master and slave (connects up to 16 links)
- Wi-Fi/Bluetooth coexistence protocol support
- Shared RF with BDR/EDR
- Encryption (AES) support
- Intelligent Adaptive Frequency Hopping (AFH)
- Bluetooth LE Privacy 1.2
- Bluetooth LE Secure Connection
- Bluetooth LE Data Length Extension
- Bluetooth LE Advertising Extension
- 2 Mbit/s Bluetooth LE

4.3 Bluetooth host interfaces

- SDIO 3.0
- High-speed UART

4.4 Coexistence

- Internal coexistence arbitration for Wi-Fi/Bluetooth

4.5 PCM interface

- Master or slave mode
- PCM bit width size of 8 bits or 16 bits
- Up to 4 slots with configurable bit width and start positions
- PCM short frame and long frame[1] synchronization
- Tri-state PCM interface capability

1 In PCM Master mode, PCM long frame synchronization is 1 clock wide. In PCM Slave mode, PCM Master's long frame synchronization pattern is supported.

5 Pin information

5.1 Signal diagrams

5.1.1 SIgnal diagram for QFN package option

Figure 6 shows the signals for the QFN package of the device.

Note: *Signals may be muxed. See Section 5.5 "Pin description".*

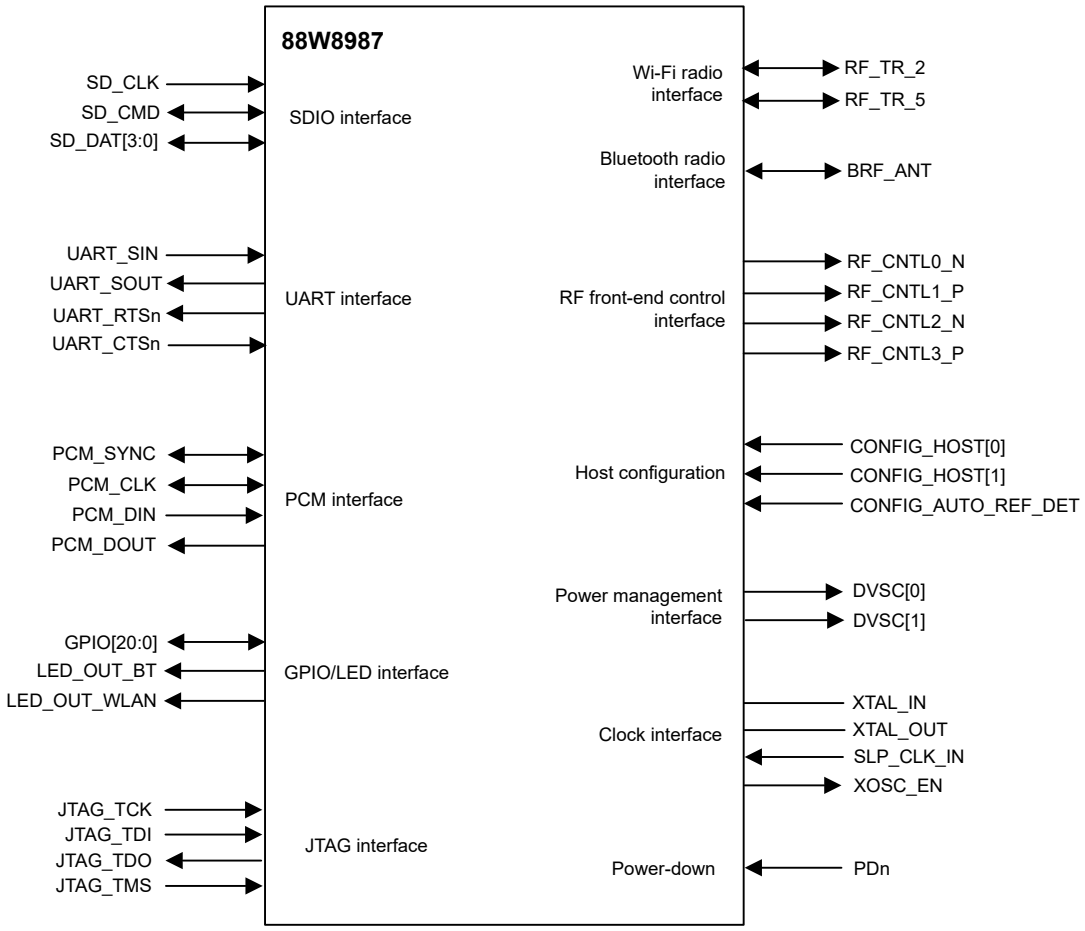


Figure 6. Signal diagram—QFN

5.1.2 Signal diagram for eWLP package option

Figure 7 shows the signals for eWLP package option.

Note: *Signals may be muxed. See* Section 5.5 "Pin description".

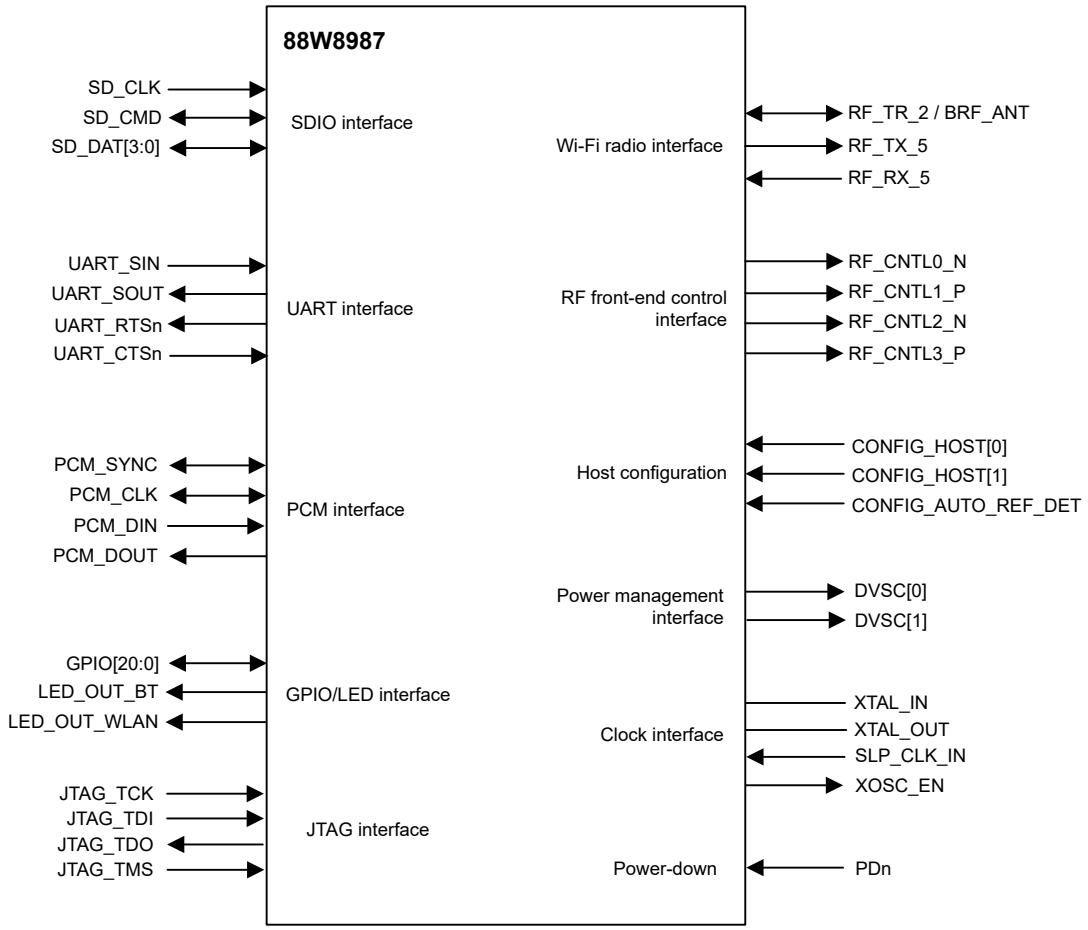


Figure 7. Signal diagram—eWLP

5.2 Pin types

Table 2. Pin types

Pin type	Description
I/O	Digital input/output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output
A, I/O	Analog input/output
NC	No connect
DNC	Do not connect
Power	Power
Ground	Ground

5.3 Pin assignment—68-pin QFN

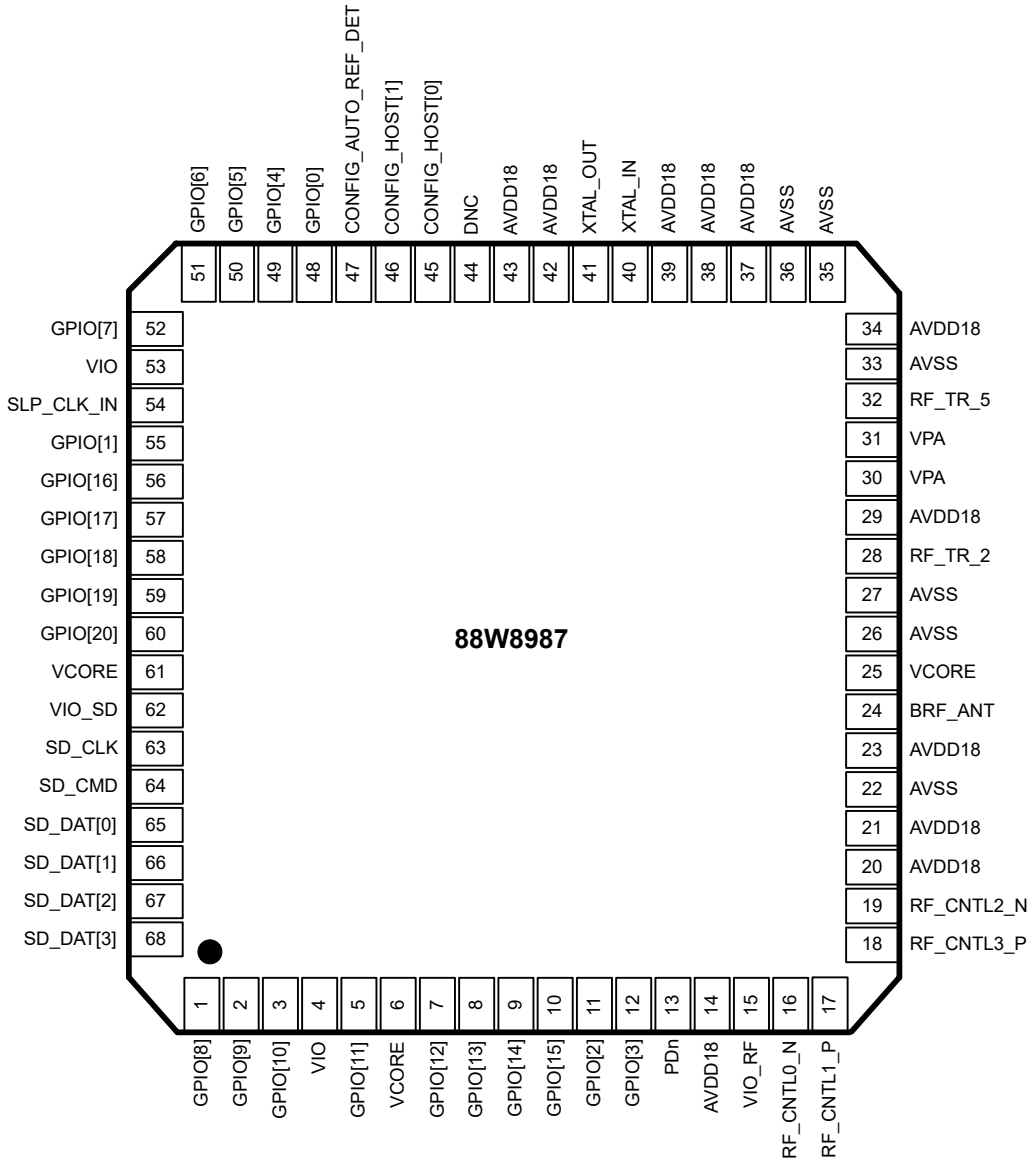


Figure 8. Pin assignment—68-pin QFN package option[1]

[1] EPAD on pin 69.

5.3.1 Pin list by number

The following table shows the pin list sorted by pin number.

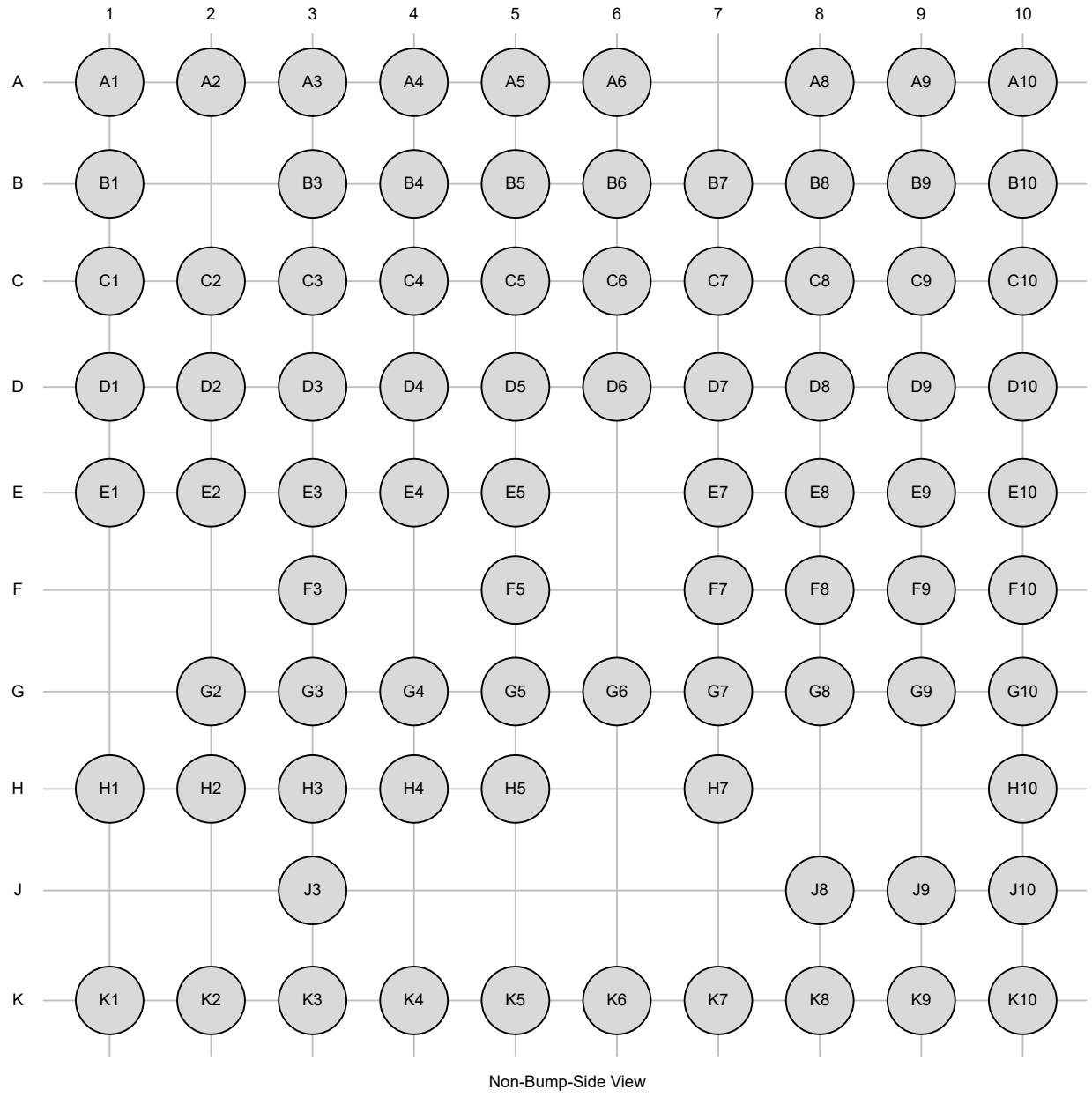
Table 3. Pin list by number

Pin number	Pin name	Power	Type
1	GPIO[8]	VIO	I/O
2	GPIO[9]	VIO	I/O
3	GPIO[10]	VIO	I/O
4	VIO	--	Power
5	GPIO[11]	VIO	I/O
6	VCORE	--	Power
7	GPIO[12]	VIO	I/O
8	GPIO[13]	VIO	I/O
9	GPIO[14]	VIO	I/O
10	GPIO[15]	VIO	I/O
11	GPIO[2]	VIO	I/O
12	GPIO[3]	VIO	I/O
13	PDn	AVDD18	I
14	AVDD18	--	Power
15	VIO_RF	--	Power
16	RF_CNTL0_N	VIO_RF	O
17	RF_CNTL1_P	VIO_RF	O
18	RF_CTLN3_P	VIO_RF	O
19	RF_CTLN2_N	VIO_RF	O
20	AVDD18	--	Power
21	AVDD18	--	Power
22	AVSS	--	Ground
23	AVDD18	--	Power
24	BRF_ANT	AVDD18	A, I/O
25	VCORE	--	Power
26	AVSS	--	Ground
27	AVSS	--	Ground
28	RF_TR_2	AVDD18	A, I/O
29	AVDD18	--	Power
30	VPA	--	Power
31	VPA	--	Power
32	RF_TR_5	AVDD18	A, I/O
33	AVSS	--	Ground
34	AVDD18	--	Power

Table 3. Pin list by number*...continued*

Pin number	Pin name	Power	Type
35	AVSS	--	Ground
36	AVSS	--	Ground
37	AVDD18	--	Power
38	AVDD18	--	Power
39	AVDD18	--	Power
40	XTAL_IN	AVDD18	I
41	XTAL_OUT	AVDD18	O
42	AVDD18	--	Power
43	AVDD18	--	Power
44	DNC	--	--
45	CONFIG_HOST[0]	AVDD18	I
46	CONFIG_HOST[1]	AVDD18	I
47	CONFIG_AUTO_REF_DET	AVDD18	I
48	GPIO[0]	VIO	I/O
49	GPIO[4]	VIO	I/O
50	GPIO[5]	VIO	I/O
51	GPIO[6]	VIO	I/O
52	GPIO[7]	VIO	I/O
53	VIO	--	Power
54	SLP_CLK_IN	VIO	I
55	GPIO[1]	VIO	I/O
56	GPIO[16]	VIO	I/O
57	GPIO[17]	VIO	I/O
58	GPIO[18]	VIO	I/O
59	GPIO[19]	VIO	I/O
60	GPIO[20]	VIO	I/O
61	VCORE	--	Power
62	VIO_SD	--	Power
63	SD_CLK	VIO_SD	I
64	SD_CMD	VIO_SD	I/O
65	SD_DAT[0]	VIO_SD	I/O
66	SD_DAT[1]	VIO_SD	I/O
67	SD_DAT[2]	VIO_SD	I/O
68	SD_DAT[3]	VIO_SD	I/O

5.4 Pad locations—83-bump eWLP



Alphanumeric designations are approximations to the grid.

Figure 9. Pad locations—83-bump eWLP (non-bump-side view, bumps down)

Table 4 indicates the pad locations in 83-bump eWLP package.

Note: *Alphanumeric designations are approximations to the grid shown in* Figure 9

Table 4. Pad locations—83-bump eWLP

Signal name	Alpha-numeric designation	Pad location relative to die center (non-bump-side view)	
		X	Y
NC	A1	-1800.0	1800.0
GPIO[18]	A2	-1400.0	1800.0
VSS	A3	-1000.0	1800.0
GPIO[19]	A4	-600.0	1800.0
VCORE	A5	-200.0	1800.0
VIO_SD	A6	200.0	1800.0
VSS	A8	1000.0	1800.0
SD_DAT[3]	A9	1400.0	1800.0
VSS	A10	1800.0	1800.0
VIO	B1	-1800.0	1400.0
SLP_CLK_IN	B3	-1000.0	1400.0
GPIO[16]	B4	-600.0	1400.0
GPIO[17]	B5	-200.0	1400.0
GPIO[20]	B6	200.0	1400.0
SD_CLK	B7	600.0	1400.0
SD_DAT[0]	B8	1000.0	1400.0
SD_DAT[1]	B9	1400.0	1400.0
SD_DAT[2]	B10	1800.0	1400.0
AVDD18	C1	-1800.0	1000.0
AVSS	C2	-1400.0	1000.0
GPIO[0] / XOSC_EN	C3	-1000.0	1000.0
GPIO[6]	C4	-600.0	1000.0
GPIO[7]	C5	-200.0	1000.0
GPIO[1]	C6	200.0	1000.0
SD_CMD	C7	600.0	1000.0
GPIO[10]	C8	1000.0	1000.0
GPIO[8]	C9	1400.0	1000.0
VIO	C10	1800.0	1000.0
XTAL_IN	D1	-1800.0	600.0
XTAL_OUT	D2	-1400.0	600.0
DNC	D3	-1000.0	600.0
CONFIG_HOST[0]	D4	-600.0	600.0
GPIO[4]	D5	-200.0	600.0
GPIO[5]	D6	200.0	600.0

Table 4. Pad locations—83-bump eWLP*...continued*

Signal name	Alpha-numeric designation	Pad location relative to die center (non-bump-side view)	
		X	Y
GPIO[12]	D7	600.0	600.0
GPIO[9]	D8	1000.0	600.0
GPIO[11]	D9	1400.0	600.0
VCORE	D10	1800.0	600.0
AVDD18	E1	-1800.0	200.0
AVSS	E2	-1400.0	200.0
AVDD18	E3	-1000.0	200.0
AVSS	E4	-600.0	200.0
CONFIG_AUTO_REF_DET	E5	-200.0	200.0
GPIO[13]	E7	600.0	200.0
GPIO[3]	E8	1000.0	200.0
GPIO[15]	E9	1400.0	200.0
GPIO[14]	E10	1800.0	200.0
AVSS	F3	-1000.0	-200.0
CONFIG_HOST[1]	F5	-200.0	-200.0
GPIO[2]	F7	600.0	-200.0
PDn	F8	1000.0	-200.0
AVDD18	F9	1400.0	-200.0
VSS	F10	1800.0	-200.0
AVDD18	G2	-1400.0	-600.0
AVSS	G3	-1000.0	-600.0
VCORE	G4	-600.0	-600.0
AVSS	G5	-200.0	-600.0
RF_CNTL0_N	G6	200.0	-600.0
RF_CNTL1_P	G7	600.0	-600.0
RF_CNTL3_P	G8	1000.0	-600.0
RF_CNTL2_N	G9	1400.0	-600.0
VIO_RF	G10	1800.0	-600.0
AVSS	H1	-1800.0	-1000.0
AVSS	H2	-1400.0	-1000.0
AVSS	H3	-1000.0	-1000.0
AVSS	H4	-600.0	-1000.0
AVSS	H5	-200.0	-1000.0
AVSS	H7	600.0	-1000.0

Table 4. Pad locations—83-bump eWLP*...continued*

Signal name	Alpha-numeric designation	Pad location relative to die center (non-bump-side view)	
		X	Y
AVSS	H10	1800.0	-1000.0
VPA	J3	-1000.0	-1400.0
AVSS	J8	1000.0	-1400.0
AVSS	J9	1400.0	-1400.0
AVSS	J10	1800.0	-1400.0
NC	K1	-1800.0	-1800.0
RF_RX_5	K2	-1400.0	-1800.0
RF_TX_5	K3	-1000.0	-1800.0
RF_TR_2 / BRF_ANT	K4	-600.0	-1800.0
AVDD18	K5	-200.0	-1800.0
AVSS	K6	200.0	-1800.0
AVDD18	K7	600.0	-1800.0
AVDD18	K8	1000.0	-1800.0
AVDD18	K9	1400.0	-1800.0
NC	K10	1800.0	-1800.0

5.5 Pin description

5.5.1 Pin states

The pin states information provided in the tables includes:

- **No Pad Power State** indicates the state when there is no power.
- **PwrDwn State** denotes the power-down state in default configuration. Many pads have programmable power-down values, which can be set by firmware.
- **Reset State** is the state after the power-on-reset state and before the hardware state (HW State).
- **HW State** (hardware state) is the state after boot code finishes and before firmware download begins (firmware may change the pin state). HW State may differ based on the pin muxing/strap setting. For example, for UART_RTSn and UART_SOUT, the boot code will enable the UART interface when the device is in SDIO-UART mode, making the HW states output high and output low, respectively.
- **PwrDwn Prog** indicates if the power-down state can be programmed.
- **PU** denotes whether the pull-up can be programmed or not.
- **PD** denotes whether the pull-down can be programmed or not.
- Pull-up and pull-down are only effective when the pad is in input mode.
- After firmware is downloaded, the pads (GPIO, RF control, and so on) are programmed in functional mode per the functionality of the pins.

5.5.2 General purpose I/O (GPIO)

Table 5. General purpose I/O (GPIO)[1] (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State[2]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[20]	VIO	tristate	output	output high[3]	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[20] (input/output). This pin can be used for Bluetooth to host wake-up (out-of-band wake-up signal)									
GPIO[19]	VIO	tristate	output	output high	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[19] (input/output) **Power Management Mode**: DVSC[1] digital voltage scaling control (output)									
GPIO[18]	VIO	tristate	output	output high	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[18] (input/output) **Power Management Mode**: DVSC[0] digital voltage scaling control (output)									
GPIO[17]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[17] (input/output) **JTAG Mode**: JTAG_TDO, JTAG test data (output) This pin is used as a configuration pin: CON[9] (input). See Section 5.6 "Configuration pins".									
GPIO[16]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[16] (input/output) **JTAG Mode**: JTAG_TDI, JTAG test data (input)									

Table 5. General purpose I/O (GPIO)[1] (MFP)*...continued*

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State[2]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO[15]	VIO	tristate	input	input	output high	yes	nominal PU	yes	yes
GPIO Mode: GPIO[15] (input/output). This pin can also be used as Bluetooth independent reset. **JTAG Mode**: JTAG_TMS, JTAG controller select (input)									
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[14] (input/output) This pin can also be used as Wi-Fi independent reset. **JTAG Mode**: JTAG_TCK, JTAG test clock (input)									
GPIO[13]	VIO	tristate	input	input[4] output[5]	output high	yes	nominal PU	yes	yes
GPIO Mode: GPIO[13] (input/output) This pin can also be used for host to 88W8987 Wi-Fi wake-up (out-of-band wake-up signal).									
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[12] (input/output) This pin can also be used for host to 88W8987 Bluetooth wake-up (out-of-band wake-up signal)									
GPIO[11]	VIO	tristate	input	input[4] output[5]	output high	yes	weak PU	yes	yes
GPIO Mode: GPIO[11] (input/output) **UART Mode**: UART_RTSn (output) (active low) This pin is used as a configuration pin: CON[8] (input). See Section 5.6 "Configuration pins".									
GPIO[10]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[10] (input/output) **UART Mode**: UART_CTSn (input) (active low)									
GPIO[9]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[9] (input/output) **UART Mode**: UART_SIN (input)									
GPIO[8]	VIO	tristate	input	input[4] output[5]	output low	yes	weak PU	yes	yes
GPIO Mode: GPIO[8] (input/output) **UART Mode**: UART_SOUT (output) This pin is used as a configuration pin: CONFIG_XOSC_SEL (input). See Section 5.6 "Configuration pins".									
GPIO[7]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[7] (input/output) **PCM Mode**: PCM_SYNC (input/output) • Output if master • Input if slave									
GPIO[6]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes

Table 5. General purpose I/O (GPIO)[1] (MFP)*...continued*

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State[2]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
GPIO Mode: GPIO[6] (input/output) **PCM Mode**: PCM_CLK (input/output) • Output if master • Input if slave									
GPIO[5]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[5] (input/output) **PCM Mode**: PCM_DOUT (output) This pin is used as a configuration pin: CON[7] (input). See Section 5.6 "Configuration pins".									
GPIO[4]	VIO	tristate	input	input	tristate	yes	nominal PU	yes	yes
GPIO Mode: GPIO[4] (input/output) **PCM Mode**: PCM_DIN (input)									
GPIO[3]	VIO	tristate	output	output high[3]	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[3] (input/output) **LED Mode**: LED_OUT_BT (output)									
GPIO[2]	VIO	tristate	output	output high[3]	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[2] (input/output) **LED Mode**: LED_OUT_WLAN (output)									
GPIO[1]	VIO	tristate	input	input	tristate	yes	weak PU	yes	yes
GPIO Mode: GPIO[1] (input/output). This pin can also be used for 88W8987 Wi-Fi to host wake-up (out-of-band wake-up signal).									
GPIO[0]	VIO	tristate	output	output high	output low	yes	nominal PU	yes	no
GPIO Mode: GPIO[0] (input/output) **Oscillator Enable Mode**: XOSC_EN (output) (active high). See Section 5.5.9 "Clock interface".									

[1] Not all GPIO pins can be used for Host-to-SoC wakeup signals.
[2] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).
[3] The signal may toggle while boot code is executing.
[4] When the device is in SDIO-SDIO mode.
[5] When the device is in SDIO-UART mode.

5.5.3 Wi-Fi/Bluetooth radio interface

Table 6. Wi-Fi/Bluetooth radio interface - QFN package

Pin Name	Type	Supply	Description
RF_TR_2	A, I/O	AVDD18	Wi-Fi Transmit/Receive (2.4 GHz)
RF_TR_5	A, I/O	AVDD18	Wi-Fi Transmit/Receive (5 GHz)
BRF_ANT	A, I/O	AVDD18	Bluetooth Transmit/Receive

Table 7. Wi-Fi/Bluetooth radio interface - eWLP package option

Pin Name	Type	Supply	Description
RF_TR_2/BRF_ANT	A, I/O	AVDD18	Wi-Fi Transmit/Receive (2.4 GHz) Bluetooth Transmit/Receive (shared path for Wi-Fi and Bluetooth)
RF_RX_5	A, I	AVDD18	Wi-Fi Receive (5 GHz)
RF_TX_5	A, O	AVDD18	Wi-Fi Transmit (5 GHz)

5.5.4 Wi-Fi RF front-end control interface

Table 8. Wi-Fi RF front-end control interface

Pin Name	Supply	No Pad Power State[1]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/PD	PU	PD
RF_CNTL0_N	VIO_RF	tristate	output	output	drive low	yes	nominal PU	no	no
RF Control 0—RF Control Output Low (output)									
RF_CNTL1_P	VIO_RF	tristate	output	output	drive high	yes	weak PU	no	no
RF Control 1—RF Control Output High (output) This pin is used as a configuration pin: CON[6] (input). See Section 5.6 "Configuration pins".									
RF_CNTL2_N	VIO_RF	tristate	output	output	drive low	yes	weak PU	no	no
RF Control 2—RF Control Output Low (output)									
RF_CNTL3_P	VIO_RF	tristate	output	output	drive high	yes	weak PU	no	no
RF Control 3—RF Control Output High (output)									

[1] Maximum input voltage is 0.4V when VIO_RF has no power (or in uncertain situations).

5.5.5 SDIO host interface

Table 9. SDIO host interface

Pin Name	Supply	No Pad Power State[1]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Clock input **SDIO 1-bit Mode**: Clock input									
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Command/response (input/output) **SDIO 1-bit Mode**: Command line									
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[3] **SDIO 1-bit Mode**: Reserved									
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) **SDIO 1-bit Mode**: Read wait (optional)									
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[1] **SDIO 1-bit Mode**: Interrupt									
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	yes	yes
SDIO 4-bit Mode: Data line Bit[0] **SDIO 1-bit Mode**: Data line									

[1] Maximum input voltage is 0.4V when VIO_SD has no power (or in uncertain situations).

5.5.6 UART host interface

Table 10. UART host interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
UART_SIN	I	VIO	UART serial input signal - GPIO[9] input/output
UART_SOUT	O	VIO	UART serial output signal - GPIO[8] input/output
UART_RTSn	O	VIO	UART request-to-send output signal . Active low - GPIO[11] input/ output
UART_CTSn	I	VIO	UART clear-to-send input signal - Active low - GPIO[10] input/output

5.5.7 Audio interface

Table 11. Audio interface pins (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Type	Supply	Description
PCM_DIN	I	VIO	Receive PCM input signal. GPIO[4] input/ouput
PCM_DOUT	O	VIO	Transmit PCM output signal. GPIO[5] input/ouput
PCM_CLK	I/O	VIO	PCM data clock. GPIO[6] input/output • Output if master • Input if slave
PCM_SYNC	I/O	VIO	PCM frame sync. GPIO[7] input/ouput • Output if master • Input if slave

5.5.8 Configuration interface

Table 12. Configuration interface

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/PD	PU	PD
CONFIG_HOST[0]	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
This pin is used as a configuration pin: CONFIG_HOST[0] (input). See Section 5.6 "Configuration pins".									
CONFIG_HOST[1]	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
This pin is used as a configuration pin: CONFIG_HOST[1] (input). See Section 5.6 "Configuration pins".									
CONFIG_AUTO_REF_DET	AVDD18	tristate	input	input	tristate	no	weak PU	yes	yes
This pin is used as a configuration pin: CONFIG_AUTO_REF_DET (input). See Section 5.6 "Configuration pins".									

5.5.9 Clock interface

Table 13. Clock interface (MFP)

Pins may be Multi-Functional Pins (MFP).

Pin Name	Supply	No Pad Power State[1]	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
XTAL_IN	AVDD18	--	--	--	--	--	--	--	--
Reference Clock Input Reference clock signal frequency must be 26 MHz or 38.4 MHz from an external crystal or external crystal oscillator. Power consumption in sleep mode is lower with an external crystal compared to an external crystal oscillator when an external sleep clock is not used. See Section 9.9 "Reference clock specifications".									
XTAL_OUT	AVDD18	--	--	--	--	--	--	--	--
Connect this pin to an external crystal when an external crystal is used. When an external crystal oscillator is used, connect this pin to ground with resistance less than 5 kΩ.									
SLP_CLK_IN	VIO	tristate	input[2]	input	tristate	no	nominal PU	yes	yes
Sleep Clock Input (optional) Used for lower power operation in sleep mode. • An external sleep clock of 32.768 kHz can be used for lowest current consumption in sleep mode. • An external sleep clock is required if automatic reference clock frequency detection is used. See Section 5.6 "Configuration pins". • If no external sleep clock is used, leave this pin floating (DNC).									
XOSC_EN	VIO	--	--	--	--	--	--	--	--
Oscillator Enable (output) (active high) XOSC_EN signal can be used ONLY when an external sleep clock is used. Used to enable an external oscillator. 0 = disable external oscillator 1 = enable external oscillator NOTE: Muxed with GPIO[0].									

[1] Maximum input voltage is 0.4V when VIO has no power (or in uncertain situations).
[2] Input mode after reset

5.5.10 Power down (PDn) pin

Table 14. Power down (PDn) pin

Pin Name	Supply	No Pad Power State	Reset State	HW State	PwrDwn State	PwrDwn Prog	Internal PU/ PD	PU	PD
PDn	AVDD18	--	--	--	--	--	--	--	--
Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode • PDn can accept an input of 1.8V to 4.5V • PDn may be driven by the host • PDn must be high for normal operation No internal pull-up on this pin.									

5.5.11 Power supply and ground

Table 15. Power supply and ground

Pin Name	Type	Description
VCORE	Power	1.10V Core Power Supply
VIO	Power	1.8V/3.3V Digital I/O Power Supply
VIO_SD	Power	1.8V Digital I/O SDIO Power Supply
VIO_RF	Power	1.8V/3.3V Analog I/O RF Power Supply
AVDD18	Power	1.8V Analog Power Supply
VPA	Power	2.2V Analog Power Supply
AVSS	Ground	Ground
NC	NC	Not Connected
DNC	DNC	Do Not Connect Do not connect these pins. Leave these pins floating.

5.6 Configuration pins

Table 16 shows the pins used as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function.

To set a configuration bit to 0, attach a 50 kΩ–100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

See Section 9.11 "Configuration pin specifications" for the internal pull-up values of the configuration pins.

Table 16. Configuration pins

Configuration Bits	Pin Name	Configuration Function
CON[9]	GPIO[17]	Reserved Set to 1.
CON[8]	GPIO[11]	
CON[7]	GPIO[5]	
CON[6]	RF_CNTL1_P	Reserved Set to 1.
CONFIG_XOSC_SEL	GPIO[8]/UART_SOUT	Reference clock frequency select Valid when CONFIG_AUTO_REF_DET = 0 0 = 38.4 MHz 1 = 26 MHz (default)
CONFIG_AUTO_REF_DET	CONFIG_AUTO_REF_DET	Reference clock frequency detection select 0 = reference clock frequency detection by CONFIG_XOSC_SEL 1 = reference clock frequency detection using external sleep clock (default)(valid only when external sleep clock is used)
CON[1]	CONFIG_HOST[1]	Host configuration options No hardware impact. Software reads and boots accordingly. See Table 17.
CON[0]	CONFIG_HOST[0]	

Table 17. Host configuration options

Strap Value	Wi-Fi	Bluetooth/ Bluetooth LE	Number of SDIO Functions
00 (reserved)	--	--	--
01 (reserved)	--	--	--
10	SDIO	UART	1 (Wi-Fi)
11	SDIO	SDIO	2 (Wi-Fi, Bluetooth)

6 Power information

Section 5.5.11 "Power supply and ground" shows the required voltage levels for each rail and for PDn input signal.

6.1 Power-up sequence

- VIO/VIO_RF must be good (90%) before or at the same time all other power supplies start ramping up.
- VIO/VIO_RF must be good (90%) before or at the same time PDn starts ramping up.
- VPA must be good (90%) before or at the same time AVDD18 starts ramping up.
- It is recommended to start ramping up AVDD18 ≤1 ms after VPA ramps up.
- AVDD18 must be good (90%) before or at the same time VCORE starts ramping up.
- Ramp-up time of VIO/VIO_RF must be <100 ms.
- Ramp-up time of VPA must be <100 ms.
- Ramp-up time of AVDD18 must be <100 ms.
- Ramp-up time of VCORE must be <5 ms.
- All supplies must be monotonic.
- If using an external crystal oscillator, the reference clock must be stable before PDn ramps up.

Figure 10 shows the power-up sequence.

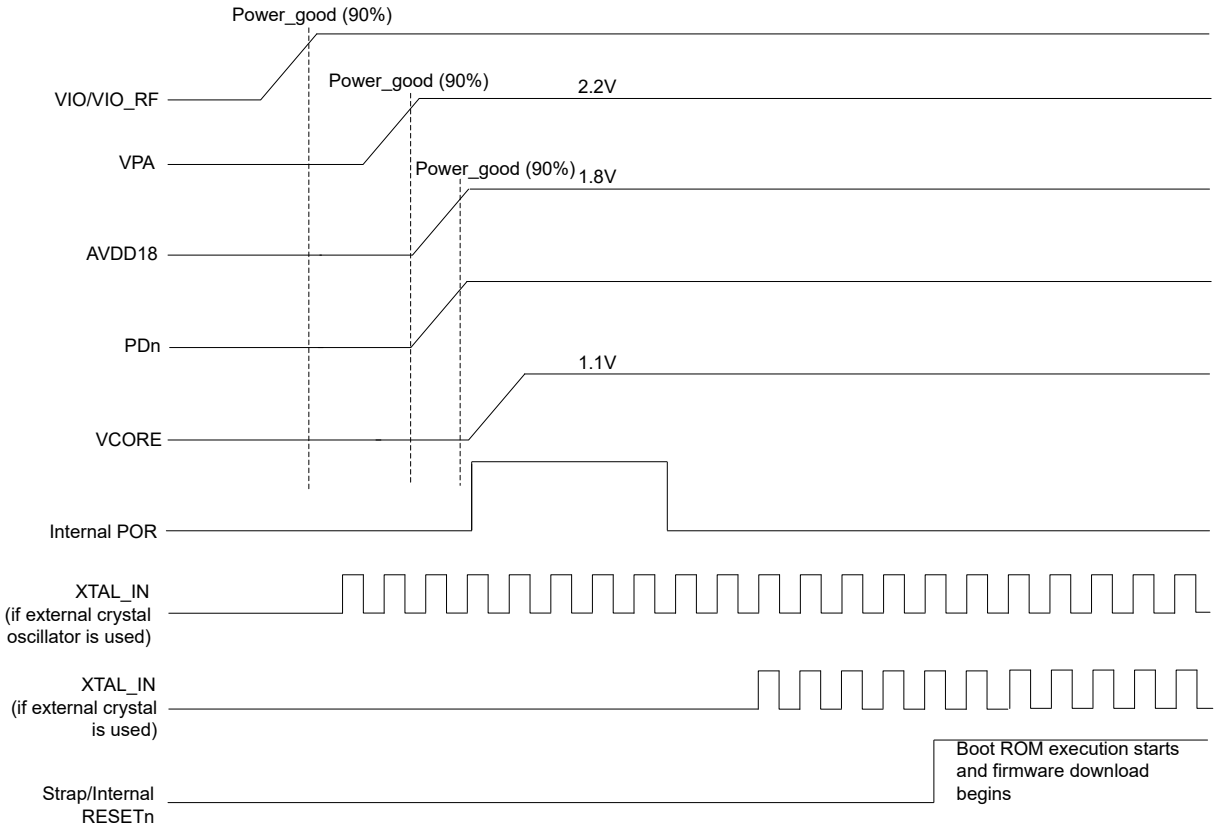


Figure 10. Power-up sequence

6.2 Power-down sequence

It is recommended:

- To ramp down AVDD18 after VPA ramps down
- To discharge all of the power supplies to less than 0.2V to reduce leakage.

PDn must be asserted when powering down the device.

Figure 11 shows the power-down sequence.

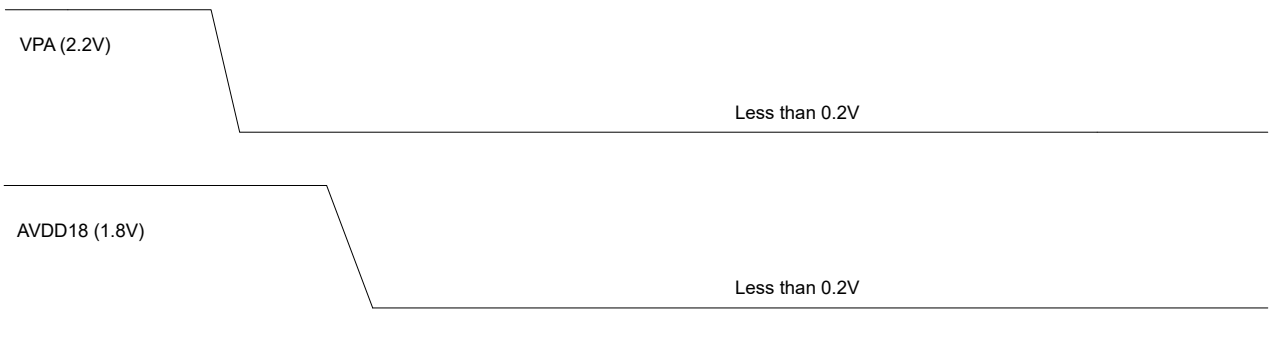


Figure 11. Power-down sequence

6.3 Reset

88W8987 is reset to its default operating state under any of the following conditions:

- Internal Power-On Reset (POR): POR is triggered when the device receives power and VCORE and AVDD18 supplies are good. See Section 6.1 "Power-up sequence".
- Software/Firmware reset: the software or firmware issues a reset.
- External PDn pin assertion: the device is reset when the PDn input pin is <0.2V and transitions from low to high.

See Section 9.10 "Power-down (PDn) pin specifications" for the electrical specifications.

6.3.1 Lowest power state

The device can be put into the lowest power mode of operation to conserve energy when Wi-Fi and Bluetooth are not in use.

To put the device in the lowest power mode, assert PDn low to enter power-down mode. Once PDn is de-asserted, the power sequence must be followed. If the firmware is not downloaded, the device must be kept in power-down mode to reduce leakage.

7 Absolute maximum ratings

CAUTION: The absolute maximum ratings table defines the limitations for electrical and thermal stresses. These limits prevent permanent damage to the device. Exposure to conditions at or beyond these ratings is not guaranteed and can damage the device.

Table 18. Absolute maximum ratings

Symbol	Parameter	Min	Max	Units
VCORE	1.10V core power supply	--	1.21	V
VIO	1.8V/3.3V digital I/O power supply	--	2.2[1]	V
		--	4.0[2]	V
VIO_SD	1.8V digital I/O SDIO power supply	--	2.2	V
VIO_RF	1.8V/3.3V I/O power supply	--	2.2[3]	V
		--	4.0[4]	V
AVDD18	1.8V analog power supply	--	1.98	V
VPA	2.2V analog power supply	--	2.3	V
$T_{STORAGE}$	Storage Temperature	-55	+125	°C

[1] When using 1.8V digital I/O power supply
[2] When using 3.3V digital I/O power supply
[3] When using 1.8V I/O power supply
[4] When using 3.3V I/O power supply

Table 19. Limiting values - QFN option

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-1.5	+1.5	kV
		charged device model (CDM)[2]	-500	+500	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

Table 20. Limiting values - eWLP option

Symbol	Parameter	Condition	Min	Max	Unit
V_{ESD}	Electrostatic discharge	human body model (HBM)[1]	-1.5	+1.5	kV
		charged device model (CDM)[2]	-400	+400	V

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002

8 Recommended operating conditions

Note: *Operation beyond the recommended operating conditions is neither recommended nor guaranteed.*

Table 21. Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCORE	1.10V core power supply	--	1.05	1.10	1.15	V
VIO	1.8V/3.3V digital I/O power supply	--	1.67	1.8	1.92	V
			3.07	3.3	3.53	V
VIO_SD	1.8V digital I/O SDIO power supply	--	1.67	1.8	1.92	V
VIO_RF	1.8V/3.3V I/O power supply	--	1.67	1.8	1.92	V
			3.07	3.3	3.53	V
AVDD18	1.8V analog power supply	--	1.71	1.8	1.89	V
VPA	2.2V analog power supply	--	2.09	2.2	2.26	V
T_A	Ambient operating temperature	Extended	-30	--	85	°C
		Industrial	-40	--	85	°C
T_J	Maximum junction temperature	--	--	--	125	°C

9 Electrical specifications

9.1 GPIO/LED interface specifications

9.1.1 VIO DC characteristics

9.1.1.1 1.8V operation

Table 22. DC electrical characteristics—1.8V operation (VIO)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

9.1.1.2 3.3V operation

Table 23. DC electrical characteristics—3.3V operation (VIO)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO	--	VIO+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

9.1.2 LED mode

Table 24. LED mode data

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Typ	Unit
I_{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I_{OL}	Switching current low	@ 0.4V	10	mA

9.2 RF front-end control interface specifications

9.2.1 VIO_RF DC characteristics

9.2.1.1 1.8V operation

Table 25. DC electrical characteristics—1.8V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

9.2.1.2 3.3V operation

Table 26. DC electrical characteristics—3.3V operation (VIO_RF)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_RF	--	VIO_RF+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_RF	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_RF-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

9.3 Wi-Fi radio specifications

9.3.1 Wi-Fi radio performance measurement

The Wi-Fi transmit/receive performance is measured either at the antenna port or at the chip port.

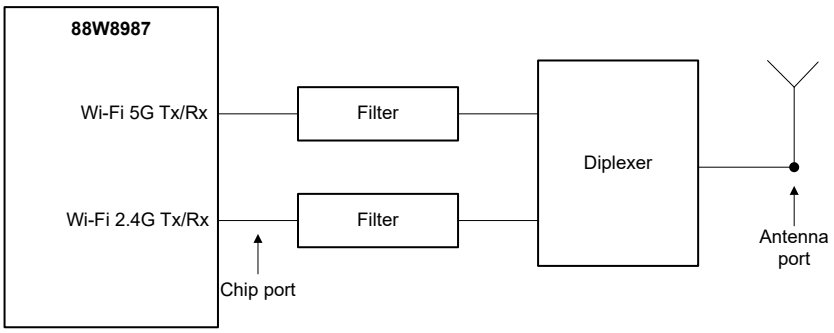


Figure 12. RF performance measurement points

9.3.2 2.4 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at chip port.*

Table 27. 2.4 GHz Wi-Fi receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	20 MHz and 40 MHz bandwidths	2400	--	2500	MHz
Rx input IP3 at RF high gain (In-Band)	Rx input IP3 when LNA in high gain mode (24 dB) at chip input	--	-20	--	dBm
Maximum Rx input level	Maximum Rx input level without device damage	--	--	2	dBm
Receiver sensitivity 802.11b	1 Mbit/s	--	-99	--	dBm
	2 Mbit/s	--	-95	--	dBm
	5.5 Mbit/s	--	-93	--	dBm
	11 Mbit/s	--	-90	--	dBm
Receiver sensitivity 802.11g	6 Mbit/s	--	-89	--	dBm
	9 Mbit/s	--	-89	--	dBm
	12 Mbit/s	--	-88	--	dBm
	18 Mbit/s	--	-87	--	dBm
	24 Mbit/s	--	-85	--	dBm
	36 Mbit/s	--	-81	--	dBm
	48 Mbit/s	--	-77	--	dBm
	54 Mbit/s	--	-76[1]	--	dBm
Receiver sensitivity 802.11n HT20[1] BCC waveform	MCS0	--	-89	--	dBm
	MCS1	--	-88	--	dBm
	MCS2	--	-85	--	dBm
	MCS3	--	-83	--	dBm
	MCS4	--	-80	--	dBm
	MCS5	--	-76	--	dBm
	MCS6	--	-74	--	dBm
	MCS7	--	-73	--	dBm
Receiver sensitivity 802.11n HT40[1] BCC waveform	MCS0	--	-87	--	dBm
	MCS1	--	-86	--	dBm
	MCS2	--	-84	--	dBm
	MCS3	--	-81	--	dBm
	MCS4	--	-77	--	dBm
	MCS5	--	-73	--	dBm
	MCS6	--	-72	--	dBm
	MCS7	--	-71	--	dBm

Table 27. 2.4 GHz Wi-Fi receiver performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Receiver maximum input level	802.11b	--	-1	--	dBm
	802.11g	--	-2	--	dBm
	802.11n MCS0-4	--	-1	--	dBm
	802.11n MCS5-6	--	-2	--	dBm
	802.11n MCS7	--	-5	--	dBm
Receiver adjacent channel interference rejection (ACI) 802.11b	1 Mbit/s	--	54	--	dB
	2 Mbit/s	--	49	--	dB
	5.5 Mbit/s	--	47	--	dB
	11 Mbit/s	--	45	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11g	6 Mbit/s	--	37	--	dB
	9 Mbit/s	--	35	--	dB
	12 Mbit/s	--	39	--	dB
	18 Mbit/s	--	36	--	dB
	24 Mbit/s	--	33	--	dB
	36 Mbit/s	--	27	--	dB
	48 Mbit/s	--	27	--	dB
	54 Mbit/s	--	24	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n, HT20	MCS0	--	37	--	dB
	MCS1	--	36	--	dB
	MCS2	--	36	--	dB
	MCS3	--	30	--	dB
	MCS4	--	28	--	dB
	MCS5	--	26	--	dB
	MCS6	--	21	--	dB
	MCS7	--	20	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n, HT40,	MCS0	--	33	--	dB
	MCS1	--	32	--	dB
	MCS2	--	29	--	dB
	MCS3	--	27	--	dB
	MCS4	--	26	--	dB
	MCS5	--	22	--	dB
	MCS6	--	19	--	dB
	MCS7	--	17	--	dB

[1] De-sense of ~2 dB at 2472 MHz

9.3.3 5 GHz Wi-Fi receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 28. 5 GHz Wi-Fi receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11ac/n/a	4900	--	5925	MHz
Rx input IP3 at RF high gain (In-Band)	Rx Input IP3 when LNA in high gain mode (24 dB) at chip input	—	-20	—	dBm
Maximum Rx input level	Maximum Rx input level without device damage	—	—	2	dBm
Receiver sensitivity 802.11a	6 Mbit/s	--	-92	--	dBm
	9 Mbit/s	--	-92	--	dBm
	12 Mbit/s	--	-91	--	dBm
	18 Mbit/s	--	-89	--	dBm
	24 Mbit/s	--	-86	--	dBm
	36 Mbit/s	--	-83	--	dBm
	48 Mbit/s	--	-78	--	dBm
	54 Mbit/s	--	-77	--	dBm
Receiver sensitivity 802.11n HT20 BCC waveform	MCS0	--	-92	--	dBm
	MCS1	--	-90	--	dBm
	MCS2	--	-87	--	dBm
	MCS3	--	-84	--	dBm
	MCS4	--	-81	--	dBm
	MCS5	--	-76	--	dBm
	MCS6	--	-75	--	dBm
	MCS7	--	-73	--	dBm
Receiver sensitivity 802.11n HT40 BCC waveform	MCS0	--	-88	--	dBm
	MCS1	--	-87	--	dBm
	MCS2	--	-84	--	dBm
	MCS3	--	-81	--	dBm
	MCS4	--	-78	--	dBm
	MCS5	--	-74	--	dBm
	MCS6	--	-73	--	dBm
	MCS7	--	-71	--	dBm

Table 28. 5 GHz Wi-Fi receiver performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Receiver sensitivity 802.11ac VHT20 BCC waveform	MCS0	--	-92	--	dBm
	MCS1	--	-90	--	dBm
	MCS2	--	-88	--	dBm
	MCS3	--	-85	--	dBm
	MCS4	--	-83	--	dBm
	MCS5	--	-80	--	dBm
	MCS6	--	-78	--	dBm
	MCS7	--	-76	--	dBm
	MCS8	--	-72	--	dBm
Receiver sensitivity 802.11ac VHT40 BCC waveform	MCS0	--	-88	--	dBm
	MCS1	--	-87	--	dBm
	MCS2	--	-85	--	dBm
	MCS3	--	-82	--	dBm
	MCS4	--	-80	--	dBm
	MCS5	--	-76	--	dBm
	MCS6	--	-75	--	dBm
	MCS7	--	-74	--	dBm
	MCS8	--	-70	--	dBm
	MCS9	--	-68	--	dBm
Receiver sensitivity 802.11ac VHT80 BCC waveform	MCS0	--	-84	--	dBm
	MCS1	--	-84	--	dBm
	MCS2	--	-82	--	dBm
	MCS3	--	-79	--	dBm
	MCS4	--	-78	--	dBm
	MCS5	--	-73	--	dBm
	MCS6	--	-72	--	dBm
	MCS7	--	-71	--	dBm
	MCS8	--	-66	--	dBm
	MCS9	--	-64	--	dBm
Receiver maximum input level	802.11a 6-36 Mbit/s	--	-3	--	dBm
	802.11a 48-54 Mbit/s	--	-5	--	dBm
	802.11n MCS0-4	--	-3	--	dBm
	802.11n MCS5	--	-4	--	dBm
	802.11n MCS6	--	-5	--	dBm
	802.11n MCS7-9	--	-8	--	dBm

Table 28. 5 GHz Wi-Fi receiver performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Receiver adjacent channel interference rejection (ACI) 802.11a	6 Mbit/s	--	34	--	dB
	9 Mbit/s	--	32	--	dB
	12 Mbit/s	--	33	--	dB
	18 Mbit/s	--	32	--	dB
	24 Mbit/s	--	29	--	dB
	36 Mbit/s	--	24	--	dB
	48 Mbit/s	--	24	--	dB
	54 Mbit/s	--	17	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n, HT20	MCS0	--	32	--	dB
	MCS1	--	31	--	dB
	MCS2	--	31	--	dB
	MCS3	--	26	--	dB
	MCS4	--	22	--	dB
	MCS5	--	20	--	dB
	MCS6	--	17	--	dB
	MCS7	--	15	--	dB
Receiver adjacent channel interference rejection (ACI) 802.11n, HT40	MCS0	--	29	--	dB
	MCS1	--	28	--	dB
	MCS2	--	28	--	dB
	MCS3	--	22	--	dB
	MCS4	--	23	--	dB
	MCS5	--	19	--	dB
	MCS6	--	18	--	dB
	MCS7	--	16	--	dB

9.3.4 2.4 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 29. 2.4 GHz Wi-Fi transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	2.4 GHz—IEEE 802.11n/g/b	2400	--	2500	MHz
	2.4 GHz—IEEE 802.11ac, bandwidth 20 MHz and bandwidth 40 MHz				
Transmitter output saturation	Saturation power at chip output	--	27	--	dBm
Transmit carrier suppression (CW)	Carrier suppression at chip output	--	-36	--	dB
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output	--	-45	--	dBc
Transmit power (EVM and mask compliant) 20 MHz	802.11b	--	22	--	dBm
	OFDM BPSK	--	21	--	dBm
	OFDM QPSK	--	21	--	dBm
	OFDM 16-QAM	--	21	--	dBm
	OFDM 64-QAM	--	21	--	dBm
Transmit power (EVM and mask compliant) 40 MHz	OFDM BPSK	--	20	--	dBm
	OFDM QPSK	--	20	--	dBm
	OFDM 16-QAM	--	20	--	dBm
	OFDM 64-QAM	--	20	--	dBm
Transmit output power level control range	--	--	22[1]	--	dB
Transmit output power control step	--	--	1[2]	--	dB
Transmit output power accuracy	--	--	1.5	--	dB
Transmit carrier suppression	802.11n HT40 MCS7 at 18 dBm	--	49	--	dB

[1] 0-22 dBm
[2] Hardware capability = 0.5 dB, software capability = 1 dB

9.3.5 5 GHz Wi-Fi transmitter performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at the chip port.*

Table 30. 5 GHz Wi-Fi transmitter performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	5 GHz—IEEE 802.11ac/n/a	4900	--	5925	MHz
Transmit output saturation	Saturation power at chip output	—	27	—	dBm
Transmit carrier suppression (CW)	Carrier suppression at chip output	—	-36	—	dB
Transmit I/Q suppression with IQ calibration	I/Q suppression at chip output	—	-45	—	dBc
Transmit power (EVM and mask compliant) 20 MHz	OFDM BPSK	--	21	--	dBm
	OFDM QPSK	--	21	--	dBm
	OFDM 16-QAM	--	21	--	dBm
	OFDM 64-QAM (MCS7)	--	21	--	dBm
	OFDM 256-QAM (MCS8)	--	20	--	dBm
Transmit power (EVM and mask compliant) 40 MHz	OFDM BPSK	--	20	--	dBm
	OFDM QPSK	--	20	--	dBm
	OFDM 16-QAM	--	20	--	dBm
	OFDM 64-QAM (MCS7)	--	20	--	dBm
	OFDM 256-QAM (MCS9)	--	18	--	dBm
Transmit power (EVM and mask compliant) 80 MHz	OFDM BPSK	--	17	--	dBm
	OFDM QPSK	--	17	--	dBm
	OFDM 16-QAM	--	17	--	dBm
	OFDM 64-QAM (MCS7)	--	17	--	dBm
	OFDM 256-QAM (MCS9)	--	15	--	dBm
Transmit output power level control range		--	21[1]	--	dB
Transmit output power control step		--	1[2]	--	dB
Transmit output power accuracy		--	1.5	--	dB
Transmit carrier suppression	802.11ac MCS9 VHT80, at 15 dBm	--	51	--	dBc

[1] 0-21 dBm
[2] Hardware capability = 0.5 dB, software capability = 1 dB

9.3.6 Local oscillator

Table 31. Local oscillator

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Units
Phase noise	Measured at 2.438 GHz at 100 kHz offset	--	-103	--	dBc/Hz
Phase noise	Measured at 5.501 GHz at 100 kHz offset	—	-100	—	dBc/Hz
Integrated RMS phase noise at RF output (from 1 kHz–10 MHz)	Reference clock frequency = 38.4 MHz (2.4 GHz)	--	0.3	--	degrees
Integrated RMS phase noise at RF output (from 10 kHz–10 MHz)	Reference clock frequency = 38.4 MHz (5 GHz)	—	0.5	—	degrees
Frequency resolution	—	0.02	—	—	kHz

9.4 Bluetooth radio specifications

The Bluetooth radio interface pin is powered by AVDD18 voltage supply.

9.4.1 Bluetooth and Bluetooth LE receiver performance

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.*

Table 32. Bluetooth and Bluetooth LE receiver performance

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	--	2.4	--	2.5	GHz
IF frequency	--	--	2	--	MHz
Input IP3 (@ maximum gain of 72 dB)	--	--	-19	--	dBm
In-band blocking	**GFSK** C/I (Co-channel)	--	10	--	dB
	C/I (1 MHz)	--	-4	--	dB
	C/I (2 MHz)	--	-45	--	dB
	C/I (3 MHz)	--	-49	--	dB
	C/I (Image)	--	-21	--	dB
	C/I (Image ±1 MHz)	--	-32	--	dB
	Pi/4-DQPSK C/I (Co-channel)	--	10	--	dB
	C/I (1 MHz)	--	-9	--	dB
	C/I (2 MHz)	--	-47	--	dB
	C/I (3 MHz)	--	-51	--	dB
	C/I (Image)	--	-19	--	dB
	C/I (Image ±1 MHz)	--	-35	--	dB
	8-DPSK C/I (Co-channel)	--	16	--	dB
	C/I (1 MHz)	--	-6	--	dB
	C/I (2 MHz)	--	-42	--	dB
	C/I (3 MHz)	--	-48	--	dB
	C/I (Image)	--	-12	--	dB
	C/I (Image ±1 MHz)	--	-33	--	dB
Out-of-band blocking	30–2000 MHz	--	-12.5	--	dBm
	2–2.399 GHz	--	-12.4	--	dBm
	2.484–3 GHz	--	-18	--	dBm
	3–12.75 GHz	--	-2.6	--	dBm
RSSI range	Resolution = 1 dB	--	-90	0	dBm
50 Ω return loss	--	--	--	-10	dB

Table 32. Bluetooth and Bluetooth LE receiver performance*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
Bluetooth sensitivity (RCV/CA/01/C & RCV/CA/02/C & RCV/CA/07/C)	DH5	--	-96[1]	--	dBm
	2DH5	--	-95[2]	--	dBm
	3DH5	--	-88[3]	--	dBm
Bluetooth LE sensitivity (RCV-LE/CA/02/C)	Bluetooth LE 1 Mbit/s	--	-99[4]	--	dBm
	Bluetooth LE 2 Mbit/s	--	-96[4]	--	dBm

[1] Desense of ~9.5 dB at CH 2419 MHz, ~6 dB at 2457 MHz, ~9 dB at 2458 MHz due to internal clock harmonics
[2] Desense of ~8.5 dB at CH 2419 MHz, ~3 dB at CH 2432 MHz, ~5 dB at 2457 MHz, ~7.5 dB at 2458 MHz due to internal clock harmonics
[3] Desense of ~9 dB at CH 2419 MHz, ~3.5dB at CH 2432 MHz,~4.5 dB at 2457 MHz, ~7.5 dB at 2458 MHz due to internal clock harmonics
[4] Desense of ~7 dB at CH 2432 MHz and ~9 dB at 2458MHz due to internal clock harmonics

9.4.2 Bluetooth and Bluetooth LE transmitter performance

Note: Unless otherwise stated, all specifications are at 25°C, nominal voltage, and at BRF_ANT pin.

Table 33. Bluetooth and Bluetooth LE transmitter

Parameter	Conditions	Min	Typ	Max	Unit
RF frequency range	--	2.4	--	2.5	GHz
Gain range	Class 1 without external PA	--	30	--	dB
Gain resolution	--	--	0.5	--	dB
Spurious emission (BDR) (in-band)	±500 kHz	--	--	-20	dBc
	±2 MHz	--	-33	-20	dBm
	±3 MHz	--	-45	-40	dBm
Spurious emission (EDR) (in-band)	±1 MHz	--	--	-26	dBc
	±1.5 MHz	--	--	-20	dBm
	±2.5 MHz	--	--	-40	dBm
Spurious emission (out-of-band)	30–88 MHz	--	-65	-41.25	dBm
	88–960 MHz	--	-65	-41.25	
	0.96–20 GHz All frequencies in this range < -41.25 dBm, except at 2x Bluetooth channel frequency. Measured at pin without external filter.	--	-35	-25	
	Restricted—2.38–2.39 GHz	--	-55	-41.25	
	Restricted—2.4835–2.6 GHz	--	-50	-41.25	
Out-of-band/ Cellular band noise	GSM850 (869–894 MHz)	--	-140	--	dBm/Hz
	GSM900 (925–960 MHz)	--	-140	--	
	GSM DCS (1805–1880 MHz)	--	-135	--	
	GSM PCS (1930–1990 MHz)	--	-135	--	
	GPS (1575.42 ±1.023 MHz)	--	-140	--	
	WCDMA Band I (2110–2170 MHz)	--	-130	--	
	WCDMA Band V (869–894 MHz)	--	-140	--	
Transmit output power (TRM/CA/01/C)	BDR	--	13	--	dBm
	EDR	--	10	--	dBm
Power control (TRM/CA/03/C)		--	5	--	dB
Frequency range (TRM/CA/04/C)	Freq Low	--	2400.9	--	MHz
	Freq High	--	2481	--	MHz
-20dB BW (TRM/CA/05/C)	DH5	--	955	--	kHz
Modulation characteristics (TRM/CA/07/C)	Delta F1 avg	--	164	--	kHz
	Delta F2 max Threshold	--	100	--	%
Modulation characteristics (TRM/CA/07/C)	Delta F2/Delta F1	--	0.9	--	--
	Delta F2 avg	--	148	--	kHz

Table 33. Bluetooth and Bluetooth LE transmitter*...continued*

Parameter	Conditions	Min	Typ	Max	Unit
ICFT (TRM/CA/08/C)	DH1	--	19	--	kHz
Carrier frequency drift (TRM/CA/09/C)	Max Drift - DH1	--	-7	--	kHz
	Drift Rate - DH1	--	-0.9	--	kHz
	Max Drift - DH3	--	-7	--	kHz
	Drift Rate - DH3	--	-1	--	kHz
	Max Drift - DH5	--	-7	--	kHz
	Drift Rate - DH5	--	-1.3	--	kHz
EDR relative power (TRM/CA/10/C)	2DH5 (DPSK/GFSK)	--	-0.1	--	dB
	3DH5 (DPSK/GFSK)	--	-0.1	--	dB
EDR carrier frequency stability and modulation accuracy (TRM/CA/11/C)	2DH5 Peak DEVM	--	0.07	--	--
	2DH5 RMS DEVM	--	0.03	--	--
	3DH5 Peak DEVM	--	0.08	--	--
	3DH5 RMS DEVM	--	0.03	--	--
Diff. phase encoding (TRM/CA/12/C)	2DH5	--	100	--	%
	3DH5	--	100	--	%
Bluetooth LE output power (TRM/-Bluetooth LE/CA/01/C)	Bluetooth LE 1 Mbit/s	--	10	--	dBm
	Bluetooth LE 2 Mbit/s	--	10	--	dBm
Bluetooth LE modulation characteristics (TRM-Bluetooth LE/CA/05/C)	Delta F1 avg - Bluetooth LE 1 Mbit/s	--	247	--	kHz
	Delta F2/Delta F1- Bluetooth LE 1 Mbit/s	--	0.9	--	kHz
	Delta F2 avg - Bluetooth LE 1 Mbit/s	--	223	--	kHz
	Delta F1 avg - Bluetooth LE 2 Mbit/s	--	504	--	kHz
	Delta F2/Delta F1- 2 Mbit/s	--	1	--	kHz
	Delta F2 avg- Bluetooth LE 2 Mbit/s	--	474	--	kHz
Bluetooth LE carrier frequency drift (TRM-Bluetooth LE/CA/06/C)	Max Drift - Bluetooth LE 1 Mbit/s	--	0.5	--	kHz
	Drift Rate - Bluetooth LE 1 Mbit/s	--	1.5	--	kHz
	Max Drift - Bluetooth LE 2 Mbit/s	--	-1.5	--	kHz
	Drift Rate - Bluetooth LE 2 Mbit/s	--	1	--	kHz
Frequency accuracy (TRM-LE/CA/BV-06-C)	Bluetooth LE 1 Mbit/s	--	-9	--	kHz
	Bluetooth LE 2 Mbit/s	--	-10	--	kHz

9.5 Current consumption

Note: *Unless otherwise stated, all specifications are at 25°C, nominal voltage, across frequency and typical value. Data is collected with SDIO-SDIO interface configuration. The power consumption in transmit mode refers to the device port pin*

Table 34. Current consumption

Mode	2.2V	1.8V	1.1V	Unit
Sleep mode current consumption				
Power down	0	0.04	2.8	mA
Wi-Fi and Bluetooth in deep- sleep mode	0	0.02	1.01	mA
Wi-Fi only in deep-sleep mode	0	0.025	1.04	mA
Bluetooth only in deep-sleep mode	0	0.024	1.14	mA
Bluetooth LE only in deep-sleep mode	0	0.02	1.22	mA
Bluetooth LE current consumption[1]				
Bluetooth LE advertise (interval = 1.28s)	0	0.05	1.1	mA
Bluetooth LE scan (interval = 1.28s, window = 11.25 ms)	0	0.15	1.2	mA
Bluetooth LE link (master mode, interval=1.28s)	0	0.07	1.2	mA
Bluetooth LE peak transmit (at 0 dBm), 1 Mbit/s	0	25	21	mA
Bluetooth LE peak transmit (at 5 dBm), 1 Mbit/s	0	37	23	mA
Bluetooth LE peak transmit (at 10 dBm), 1 Mbit/s	0	53	22	mA
Bluetooth LE peak receive, 1 Mbit/s	0	17	21	mA
Bluetooth current consumption[1]				
Bluetooth page scan	0	0.18	1.2	mA
Bluetooth page and inquiry scan	0	0.32	1.33	mA
Bluetooth ACL link, master sniff mode, (interval = 1.28s)	0	0.09	1.3	mA
Bluetooth ACL link, master sniff mode, (interval = 500 ms)	0	0.18	1.7	mA
Bluetooth ACL (data pump) DH1	0	11.7	18	mA
Bluetooth ACL (data pump) 2-DH3	0	17.2	19.5	mA
Bluetooth ACL (data pump) 3-DH5	0	19.3	20	mA
Bluetooth SCO HV3 peak transmit (at 0 dBm)	0	25	21	mA
Bluetooth SCO HV3 peak transmit (at 5 dBm)	0	37	23	mA
Bluetooth SCO HV3 peak transmit (at 10 dBm)	0	53	22	mA
Bluetooth SCO HV3 peak transmit (at 13 dBm)	0	67	22	mA
Bluetooth SCO HV3 Peak Receive	0	17	21	mA
Bluetooth Peak Transmit (at 0 dBm), DH5	0	25	21	mA
Bluetooth Peak Transmit (at 5 dBm), DH5	0	37	23	mA
Bluetooth Peak Transmit (at 10 dBm), DH5	0	53	22	mA
Bluetooth Peak Transmit (at 13 dBm), DH5	0	67	22	mA
Bluetooth Peak Receive, DH5	0	17	21	mA

Table 34. Current consumption*...continued*

Mode	2.2V	1.8V	1.1V	Unit
IEEE power save mode[2]				
IEEE-PS_2GHz-Legacy (DTIM-1)	0	1	3.18	mA
IEEE-PS_2GHz-Legacy (DTIM-3)	0	0.35	1.88	mA
IEEE-PS_2GHz-Legacy (DTIM-5)	0	0.2	1.7	mA
IEEE-PS_2GHz-Legacy (DTIM-10)	0	0.14	1.27	mA
IEEE-PS_5GHz-Legacy (DTIM-1)	0	0.7	2.33	mA
IEEE-PS_5GHz-Legacy (DTIM-3)	0	0.25	1.6	mA
IEEE-PS_5GHz-Legacy (DTIM-5)	0	0.15	1.43	mA
IEEE-PS_5GHz-Legacy (DTIM-10)	0	0.12	1.32	mA
2.4 GHz Wi-Fi receive mode[3]				
802.11b, 11 Mbit/s	0	40	95	mA
802.11g, 54 Mbit/s	0	38	112	mA
802.11n, HT20 MCS7	0	38	118	mA
5 GHz Wi-Fi 5 receive mode[3]				
802.11a, 54 Mbit/s	0	54	118	mA
802.11n, HT20 MCS7	0	55	120	mA
802.11n, HT40 MCS7	0	65	140	mA
802.11ac, VHT20 MCS8	0	55	120	mA
802.11ac, VHT40 MCS9	0	65	140	mA
802.11ac, VHT80 MCS9	0	70	158	mA
2.4 GHz Wi-Fi transmit mode[3]				
802.11b, 11 Mbit/s at 20 dBm	400	80	221	mA
802.11g, 54 Mbit/s at 20 dBm	377	79	220	mA
802.11n, HT20 MCS0 at 20 dBm	382	80	238	mA
802.11n, HT20 MCS7 at 20 dBm	382	80	238	mA
5 GHz Wi-Fi transmit mode[3]				
802.11a, 6 Mbit/s at 19 dBm	285	141	215	mA
802.11a, 54 Mbit/s at 19 dBm	285	141	220	mA
802.11n, HT20 MCS0 at 19 dBm	290	145	238	mA
802.11n, HT20 MCS7 at 19 dBm	290	145	238	mA
802.11n, HT40 MCS0 at 17 dBm	230	138	239	mA
802.11n, HT40 MCS7 at 17 dBm	230	138	239	mA
802.11ac, VHT20 MCS0 at 19 dBm	290	144	235	mA
802.11ac, VHT20 MCS8 at 19 dBm	290	144	235	mA
802.11ac, VHT40 MCS0 at 17 dBm	230	138	238	mA
802.11ac, VHT40 MCS9 at 17 dBm	230	138	238	mA

Table 34. Current consumption*...continued*

Mode	2.2V	1.8V	1.1V	Unit
802.11ac, VHT80 MCS0 at 15 dBm	190	132	232	mA
802.11ac, VHT80 MCS9 at 15 dBm	190	132	232	mA
Peak current consumption during device initialization				
Maximum peak current consumption during device initialization	975	198	198	mA

[1] Wi-Fi core in sleep mode
[2] Beacon interval = 100 ms. Bluetooth not enabled
[3] Bluetooth in deep-sleep mode

9.6 SDIO host interface specifications

The SDIO host interface pins are powered by VIO_SD voltage supply.

The SDIO electrical specifications are identical for the 4-bit SDIO and 1-bit SDIO modes.

9.6.1 VIO_SD DC characteristics

9.6.1.1 1.8V operation

Table 35. DC electrical characteristics—1.8V operation (VIO_SD)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Input high voltage	--	0.7*VIO_SD	--	VIO_SD+0.4	V
V_{IL}	Input low voltage	--	-0.4	--	0.3*VIO_SD	V
V_{HYS}	Input hysteresis	--	100	--	--	mV
V_{OH}	Output high voltage	--	VIO_SD-0.4	--	--	V
V_{OL}	Output low voltage	--	--	--	0.4	V

9.6.2 Default speed, high-speed modes

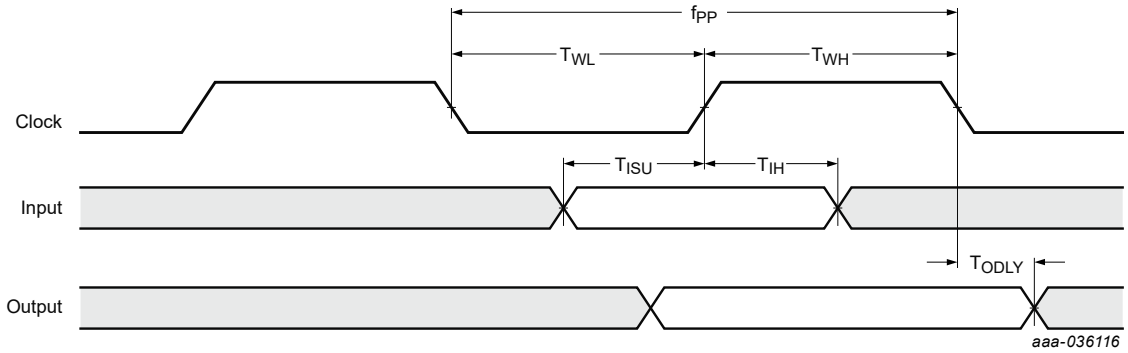


Figure 13. SDIO protocol timing diagram—Default speed mode

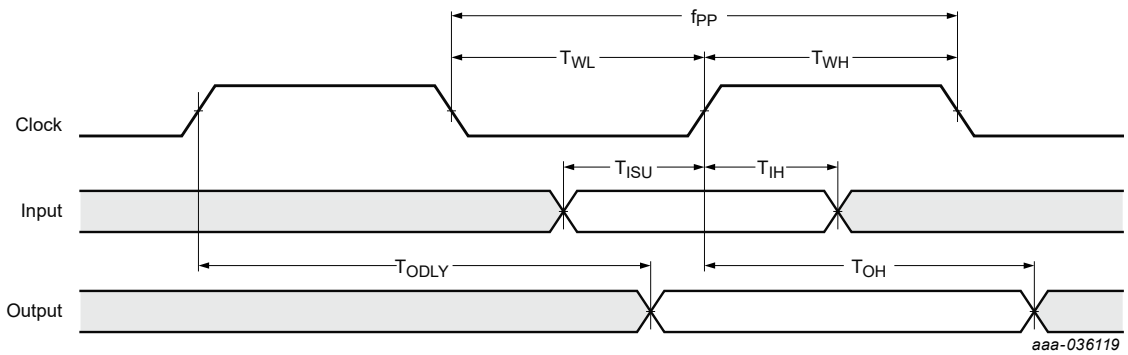


Figure 14. SDIO protocol timing diagram—High-speed mode

Table 36. SDIO timing data—Default Speed, High-Speed Modes

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	Normal	0	--	25	MHz
		High-speed	0	--	50	MHz
T_{WL}	Clock low time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{WH}	Clock high time	Normal	10	--	--	ns
		High-speed	7	--	--	ns
T_{ISU}	Input setup time	Normal	5	--	--	ns
		High-speed	6	--	--	ns
T_{IH}	Input hold time	Normal	5	--	--	ns
		High-speed	2	--	--	ns
T_{ODLY}	Output delay time	Normal	--	--	14	ns
	CL ≤ 40 pF (1 card)	High-speed	--	--	14	ns
T_{OH}	Output hold time	High-speed	2.5	--	--	ns

9.6.3 SDR12, SDR25, SDR50 modes (up to 100 MHz) (1.8V)

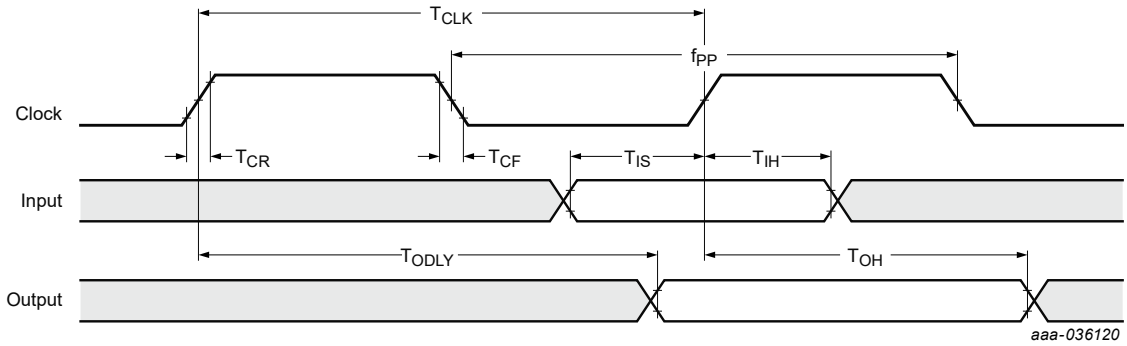


Figure 15. SDIO protocol timing diagram—SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Table 37. SDIO timing data——SDR12, SDR25, SDR50 Modes (up to 100 MHz) (1.8V)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock frequency	SDR12/25/50	25	--	100	MHz
T_{IS}	Input setup time	SDR12/25/50	3	--	--	ns
T_{IH}	Input hold time	SDR12/25/50	0.8	--	--	ns
T_{CLK}	Clock time	SDR12/25/50	10	--	40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50	--	--	0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50	--	--	7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5	--	--	ns

9.6.4 SDR104 mode (208 MHz) (1.8V)

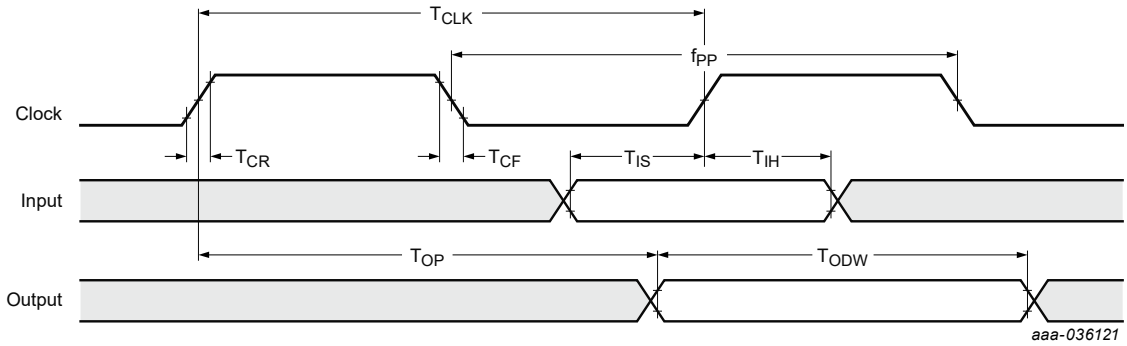


Figure 16. SDIO protocol timing diagram—SDR104 mode (208 MHz)

Table 38. SDIO timing data—SDR104 mode (208 MHz)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{PP}	Clock frequency	SDR104	0	--	208	MHz
T_{IS}	Input setup time	SDR104	1.4	--	--	ns
T_{IH}	Input hold time	SDR104	0.8	--	--	ns
T_{CLK}	Clock time	SDR104	4.8	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104	--	--	0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0	--	10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88	--	--	ns

9.6.5 DDR50 mode (50 MHz) (1.8V)

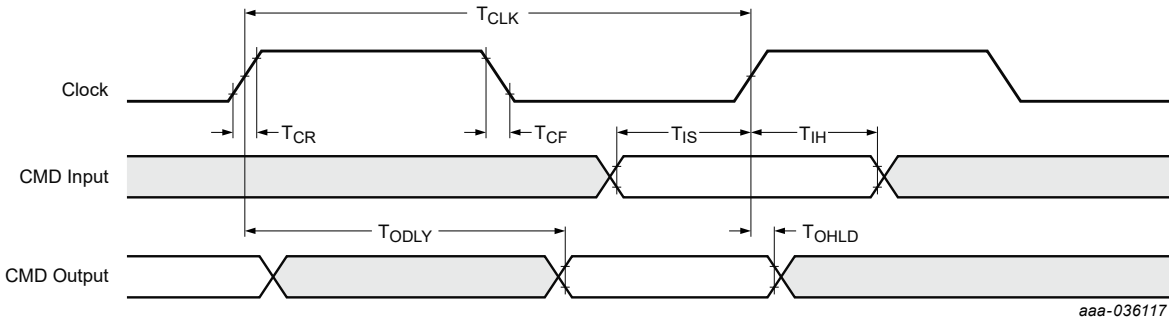


Figure 17. SDIO CMD timing diagram—DDR50 mode (50 MHz)

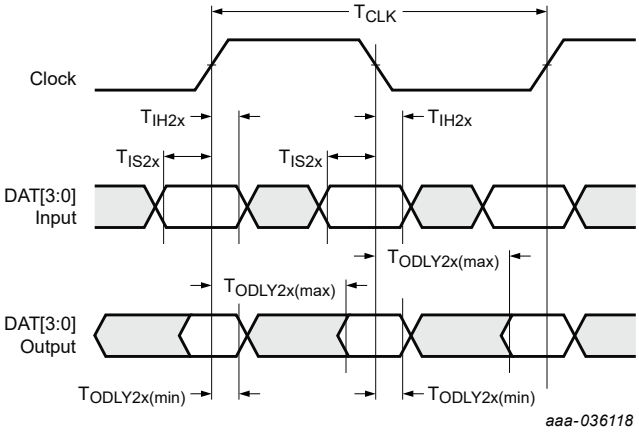


Figure 18. SDIO DAT[3:0] timing diagram—DDR50 mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Table 39. SDIO timing data—DDR50 mode (50 MHz)

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20	--	--	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50	--	--	0.2*T_{CLK}	ns
Clock Duty	--	DDR50	45	--	55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6	--	--	ns

Table 39. SDIO timing data—DDR50 mode (50 MHz)*...continued*

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50	--	--	13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3	--	--	ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8	--	--	ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50	--	--	7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5	--	--	ns

9.6.6 SDIO internal pull-up/pull-down specifications

Table 40. SDIO internal pull-up/pull-down specifications

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal nominal pull-up/pull-down resistance	--	60	90	120	kΩ

9.7 High-speed UART specifications

The UART Tx and Rx pins are powered by VIO voltage supply.

See Section 9.1.1 "VIO DC characteristics" for DC specifications.

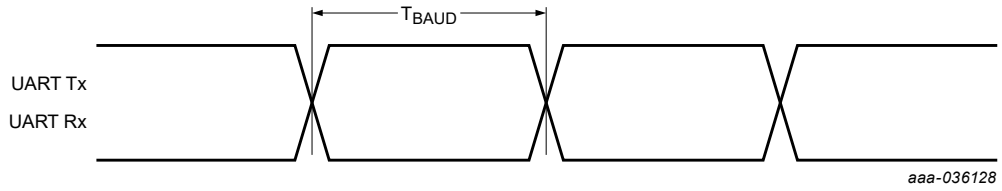


Figure 19. UART timing diagram

Table 41. UART timing data[1]

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{BAUD}	Baud rate	38.4 MHz input clock	250	--	--	ns

[1] The acceptable deviation from the UART Rx target baud rate is ±3%.

9.8 Audio interface specifications

9.8.1 PCM interface specifications

The PCM pins are powered by VIO voltage supply. See Section 9.1.1 "VIO DC characteristics" for specifications.

Master Mode

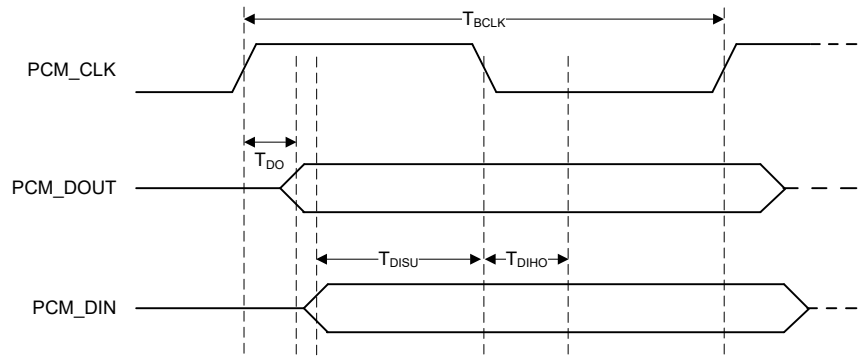


Figure 20. PCM timing specification diagram for data signals—Master mode

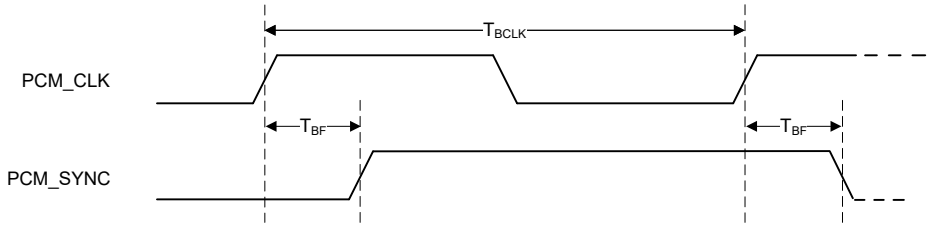


Figure 21. PCM timing specification diagram for PCM_SYNC signal—Master mode

Table 42. PCM timing specification data—Master mode

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	20	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	15	--	--	ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge	--	--	--	15	ns

Slave mode

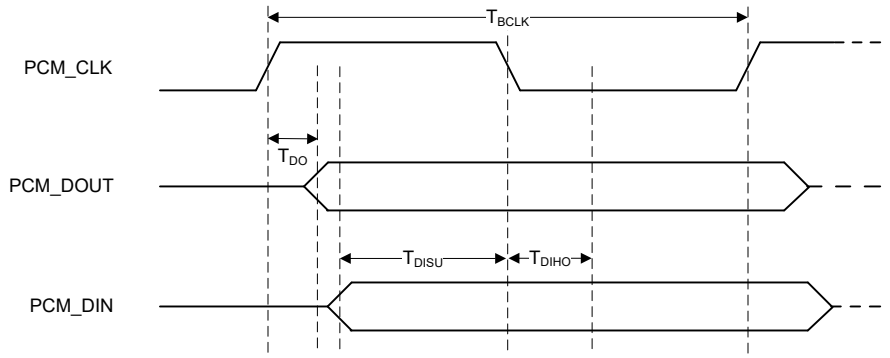


Figure 22. PCM timing specification diagram for data signals—Slave mode

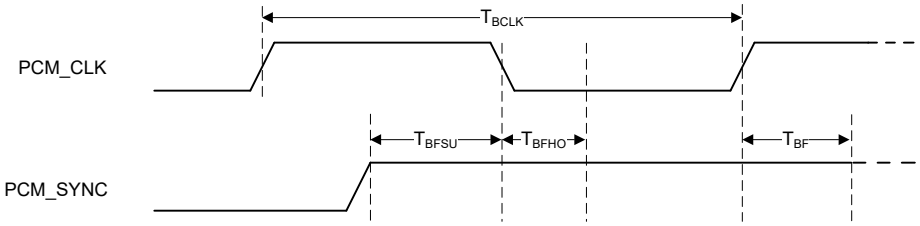


Figure 23. PCM timing specification diagram for PCM_SYNC signal—Slave mode

Table 43. PCM timing specification data—Slave mode

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{BCLK}	Bit clock frequency	--	--	2/2.048	--	MHz
Duty $Cycle_{BCLK}$	Bit clock duty cycle	--	0.4	0.5	0.6	--
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time	--	--	3	--	ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge	--	--	--	30	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge	--	15	--	--	ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge	--	10	--	--	ns
T_{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge	--	15	--	--	ns
T_{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge	--	10	--	--	ns

9.9 Reference clock specifications

9.9.1 External crystal oscillator specifications

The reference clock from the external crystal oscillator requires a CMOS input signal.

Note: *All new designs should use the 38.4 MHz reference clock. For existing designs the 26 MHz reference clock can still be used.*

Table 44. Clock DC specifications[1]

Parameter	Condition	Min	Typ	Max	Unit
Single-ended high-level voltage	--	--	--	1.8	V
Single-ended low-level voltage	--	0	--	--	V
Clock amplitude (pk-pk)	--	0.5	--	1	V
Mid-point slope	--	125	--	--	MV/s

[1] The AC-coupling capacitor is integrated into the SoC.

Table 45. 26 MHz clock timing

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO26 period	--	38.46 - 20 ppm	38.46	38.46 + 20 ppm	ns
XO26 rise time	--	--	--	5.00	ns
XO26 fall time	--	--	--	5.00	ns
XO26 duty cycle	--	48.05	50	51.95	%

Table 46. 38.4 MHz clock timing

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
XO38_4 period	--	26.04 - 20 ppm	26.04	26.04 + 20 ppm	ns
XO38_4 rise time	--	--	--	2.50	ns
XO38_4 fall time	--	--	--	2.50	ns
XO38_4 duty cycle	--	47.12	50	52.88	%

Table 47. Phase Noise—2.4 GHz operation

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-137	dBc/Hz
	Offset = 100 kHz	--	--	-145	dBc/Hz
	Offset > 1 MHz	--	--	-145	dBc/Hz
Fref = 38.4 MHz	Offset = 1 kHz	--	--	-123	dBc/Hz
	Offset = 10 kHz	--	--	-134	dBc/Hz
	Offset = 100 kHz	--	--	-142	dBc/Hz
	Offset > 1 MHz	--	--	-142	dBc/Hz

Table 48. Phase Noise—5 GHz operation

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Test Conditions	Min	Typ	Max	Unit
Fref = 26 MHz	Offset = 1 kHz	--	--	-130	dBc/Hz
	Offset = 10 kHz	--	--	-150	dBc/Hz
	Offset = 100 kHz	--	--	-156	dBc/Hz
	Offset > 1 MHz	--	--	-156	dBc/Hz
Fref = 38.4 MHz	Offset = 1 kHz	--	--	-126	dBc/Hz
	Offset = 10 kHz	--	--	-146	dBc/Hz
	Offset = 100 kHz	--	--	-154	dBc/Hz
	Offset > 1 MHz	--	--	-154	dBc/Hz

9.9.2 External crystal specifications

Note: *All new designs should use the 38.4 MHz reference clock. For existing designs the 26 MHz reference clock can still be used.*

Table 49. External crystal specifications

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Fundamental frequencies	--	--	26 or 38.4	--	MHz
Resonance mode	--	--	A1, Fundamental	--	--
Equivalent differential load capacitance	--	--	5	--	pF
Shunt capacitance	--	--	2	--	pF
Frequency tolerance	Over process at 25ºC	--	±10	--	ppm
Frequency stability	Over operating temperature	--	±10	--	ppm
Aging	--	--	±2	--	ppm/ 5 years
Series resistance (ESR)	38.4 MHz	--	--	60	Ω
	26 MHz	--	--	60	Ω
Insulation resistance	at DC 100V	500	--	--	MΩ
Drive level	--	150	--	--	µW

9.9.3 External sleep clock specifications

Table 50. External sleep clock specifications[1]

Parameter	Min	Typ	Max	Units
Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)	--	32.768	--	kHz
Phase noise requirement (@ 100 kHz)	--	-125	--	dBc/Hz
Cycle jitter	--	1.5	--	ns (RMS)
Slew rate limit (10-90%)	--	--	100	ns
Duty cycle tolerance	20	--	80	%

[1] Voltage input levels = 1.8V or 3.3V. See Section 8 "Recommended operating conditions".

9.10 Power-down (PDn) pin specifications

9.10.1 PDn asserted low—All power supplies good

Figure 24 and Table 51 show the specifications for the PDn signal when it is asserted (low) while all power supplies to the device are good.

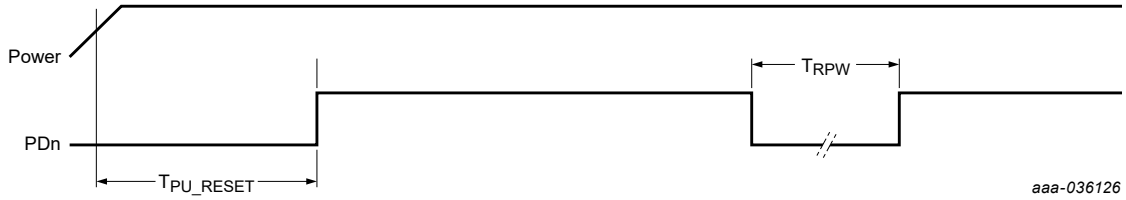


Figure 24. Power-down (PDn) pin timing—The power remains high at PDn assertion

Table 51. Power-down (PDn) pin specifications—The power remains high at PDn assertion

Unless otherwise specified, the values apply per the Recommended operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	--	0	--	--	ms
T_{RPW}	PDn pulse width	--	1[1]	--	--	µs
V_{IH}	Input high voltage	--	1.4	--	4.5	V
V_{IL}	Input low voltage	--	-0.4	--	0.5	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

9.10.2 PDn asserted Low—One or more power supplies ramp down

Figure 25 and Table 52 show the specifications for the PDn signal when it is asserted (low) while 1 or more of the power supplies (including VCORE) ramps down.

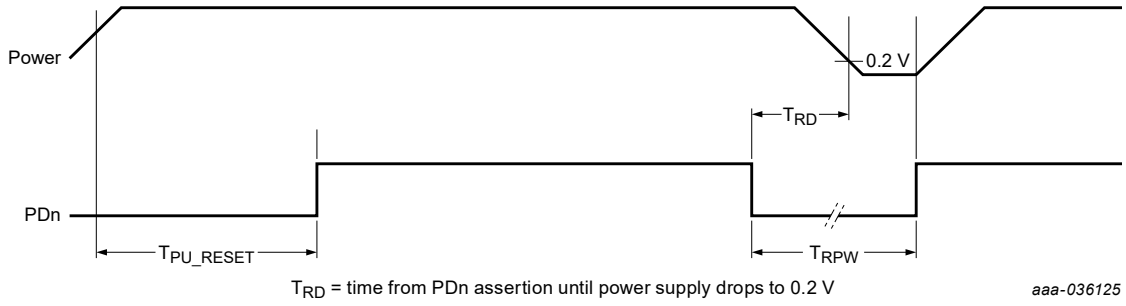


Figure 25. Power-down (PDn) pin timing—Power ramps down at PDn assertion

Table 52. Power-down (PDn) pin secifications—Power ramps down at PDn assertion

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{PU_RESET}	Valid power to PDn de-asserted	--	0	—	—	ms
T_{RPW}	PDn pulse width	--	T_{RD}[1]	—	—	µs
V_{IH}	Input high voltage	--	1.4	—	4.5	V
V_{IL}	Input low voltage	--	-0.4	—	0.2	V

[1] Minimum value guaranteed for a valid reset. Smaller values may put the device in an undefined state.

9.11 Configuration pin specifications

For a list of configuration pins, see Section 5.6 "Configuration pins".

Table 53. Configuration pin specifications[1]

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Parameter	Condition	Min	Typ	Max	Unit
Internal weak pull-up resistance	Around 1 ms following any reset	—	800	—	kΩ
Internal nominal pull-up resistance	Around 1 ms following any reset	—	100	—	kΩ

[1] After approximately 1 ms, the configuration pins become functional pins.

9.12 JTAG interface specifications

The test interface pins are powered by VIO voltage supply.

See Section 9.1.1 "VIO DC characteristics" for specifications.

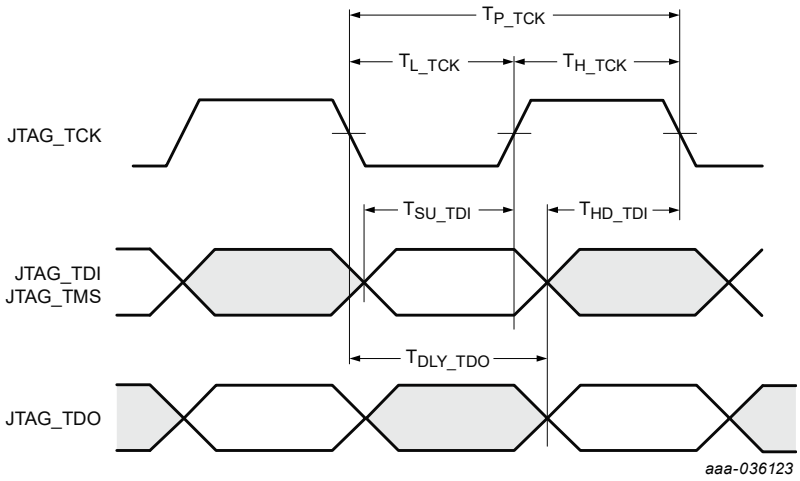


Figure 26. JTAG timing diagram

Table 54. JTAG timing data[1]

Unless otherwise specified, the values apply per Section 8 "Recommended operating conditions"

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_TCK}	TCK period	--	40	--	--	ns
T_{H_TCK}	TCK high	--	12	--	--	ns
T_{L_TCK}	TCK low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK setup time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK hold time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO delay	--	0	--	15	ns

[1] Does not apply to JTAG enabled by the JTAG_TMS pin.

10 Package information

10.1 Package thermal conditions

10.1.1 68-pin QFN thermal conditions

Table 55. Thermal conditions—QFN package

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	24 x 30 x 1.05 mm 6-layer PCB no air flow	43.00	°C/W
		24 x 30 x 1.05 mm 6-layer PCB 1 meter/sec air flow	36.90	°C/W
		24 x 30 x 1.05 mm 6-layer PCB 2 meter/sec air flow	32.50	°C/W
		24 x 30 x 1.05 mm 6-layer PCB 3 meter/sec air flow	30.30	°C/W
ψ_{JT}	Thermal characteristic parameter Junction to top-center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top-center of package	24 x 30 x 1.05 mm 6-layer PCB no air flow	4.10	°C/W
ψ_{JB}	Thermal characteristic parameter Junction to bottom surface, center of package. $\psi_{JB} = (T_J - T_B)/P$ T_B = surface temperature of package	24 x 30 x 1.05 mm 6-layer PCB no air flow	13.80	°C/W
θ_{JC}	Thermal resistance Junction to case of the package. $\theta_{JC} = (T_J - T_C)/ P_{TOP}$ T_C = temperature on top-center of package P_{TOP} = power dissipation from top of package	24 x 30 x 1.05 mm 6-layer PCB no air flow	13.80	°C/W
θ_{JB}	Thermal resistance Junction to board of package. $\theta_{JB} = (T_J - T_B)/ P_{BOTTOM}$ P_{BOTTOM} = power dissipation from bottom of package to PCB surface	24 x 30 x 1.05 mm 6-layer PCB no air flow	14.10	°C/W

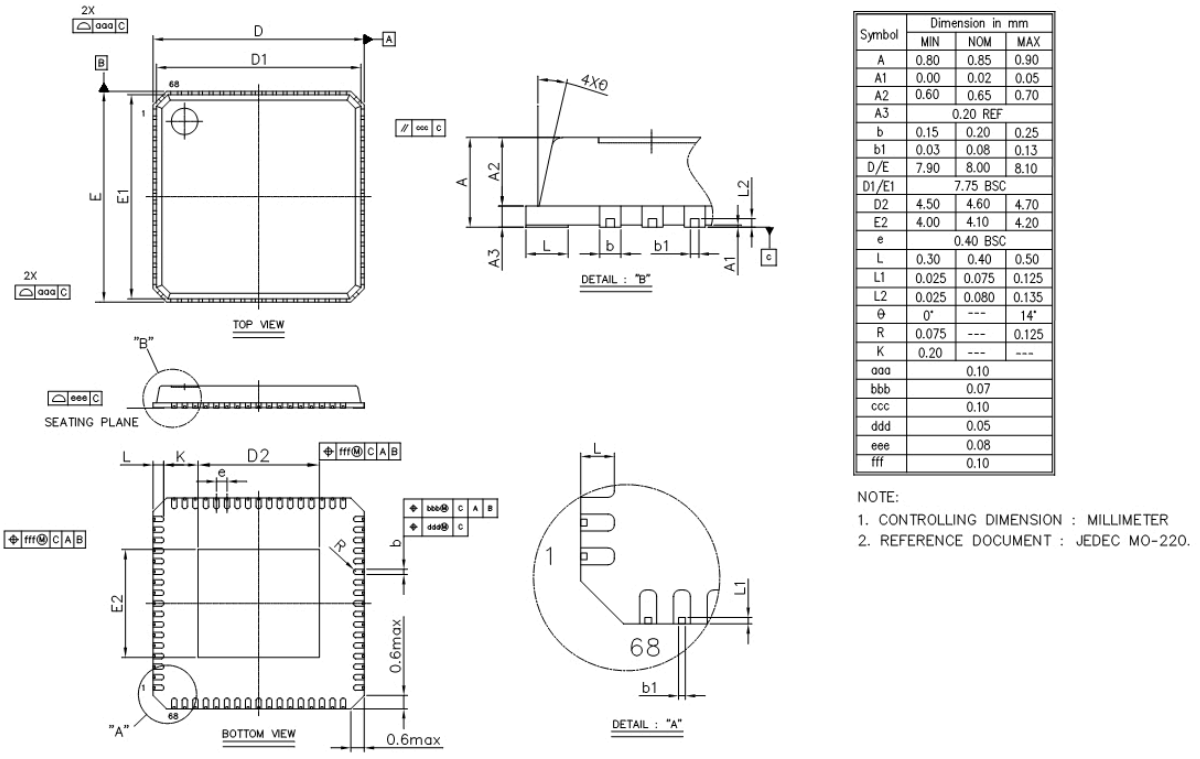
10.1.2 83-bump eWLP thermal conditions

Table 56. Thermal conditions—eWLP package

Symbol	Parameter	Condition	Typ	Unit
θ_{JA}	Thermal resistance Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 4 in. x 4.5 in. 4-layer PCB with 41 thermal via no air flow	28.07	°C/W
		JEDEC 4 in. x 4.5 in. 4-layer PCB with no thermal via no air flow	41.96	°C/W
ψ_{JT}	Thermal characteristic parameter Junction to top-center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top-center of package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no thermal via no air flow	0.08	°C/W
ψ_{JB}	Thermal characteristic parameter Junction to bottom surface, center of package. $\psi_{JB} = (T_J - T_B)/P$ T_B = surface temperature of package	JEDEC 4 in. x 4.5 in. 4-layer PCB with no thermal via no air flow	15.30	°C/W

10.2 Package mechanical drawing

10.2.1 68-pin QFN mechanical drawing



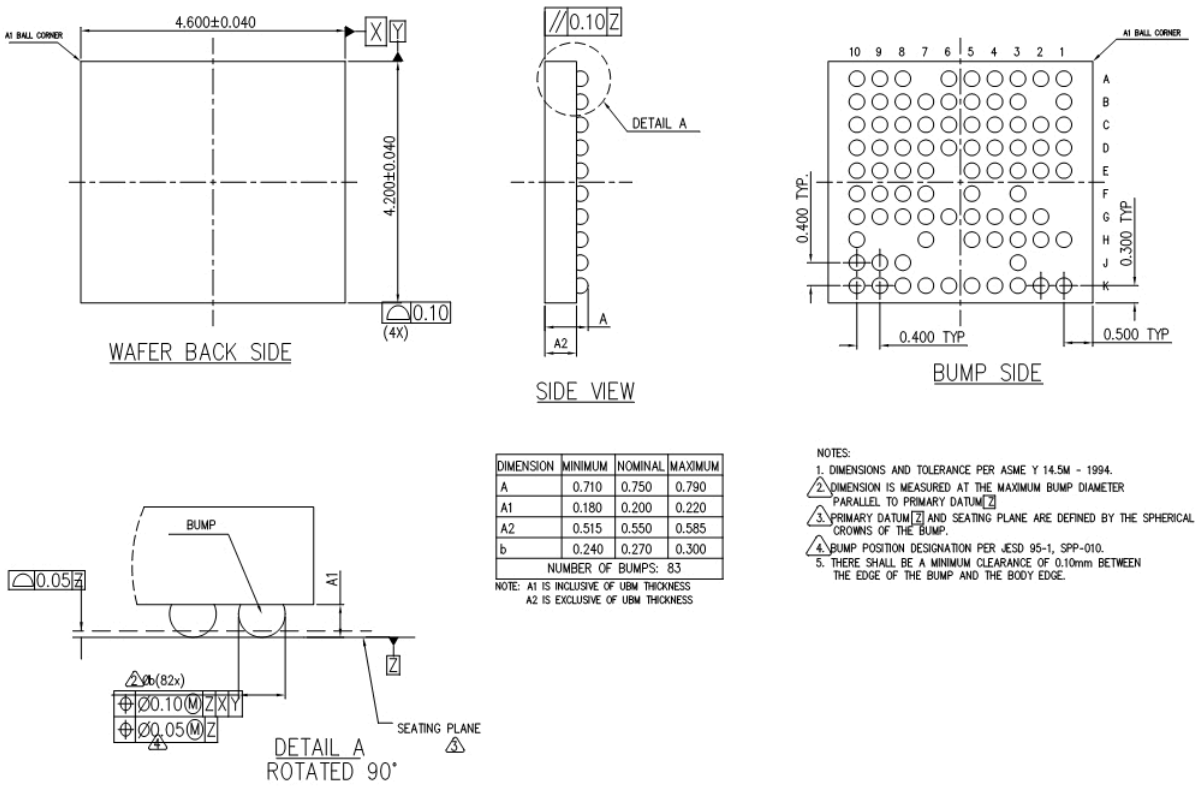
Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
b1	0.03	0.08	0.13
D/E	7.90	8.00	8.10
D1/E1		7.75 BSC	
D2	4.50	4.60	4.70
E2	4.00	4.10	4.20
e		0.40 BSC	
L	0.30	0.40	0.50
L1	0.025	0.075	0.125
L2	0.025	0.080	0.135
θ	0°	---	14°
R	0.075	---	0.125
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Figure 27. 68-pin QFN mechanical drawing

Note: *See also* Section 10.1.1 "68-pin QFN thermal conditions" *and* Section 10.3.1 "68-pin QFN package marking".

10.2.2 83-bump eWLP mechanical drawing



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.710	0.750	0.790
A1	0.180	0.200	0.220
A2	0.515	0.550	0.585
b	0.240	0.270	0.300
NUMBER OF BUMPS: 83			

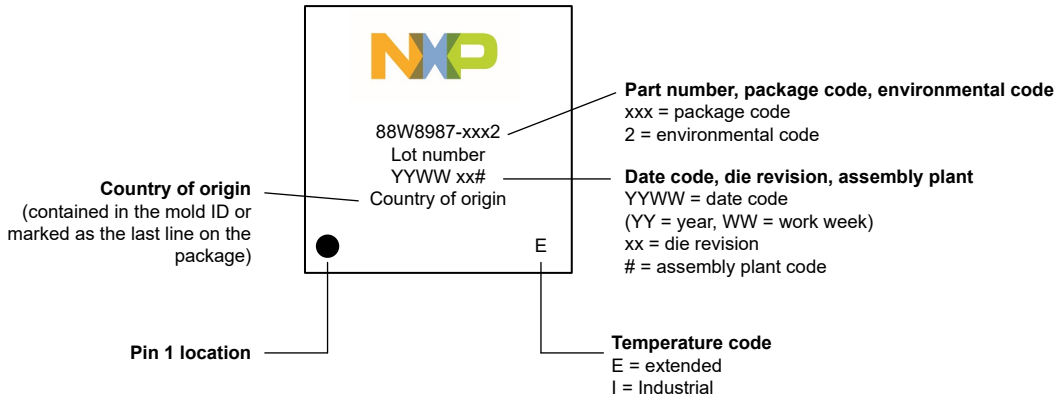
NOTE: A1 IS INCLUSIVE OF UBM THICKNESS
A2 IS EXCLUSIVE OF UBM THICKNESS

Figure 28. 83-bump eWLP mechanical drawing

- Dimensions in mm. Also refer to Section 10.1.2 "83-bump eWLP thermal conditions" and Section 10.3.2 "83-bump eWLP package marking".

10.3 Package marking

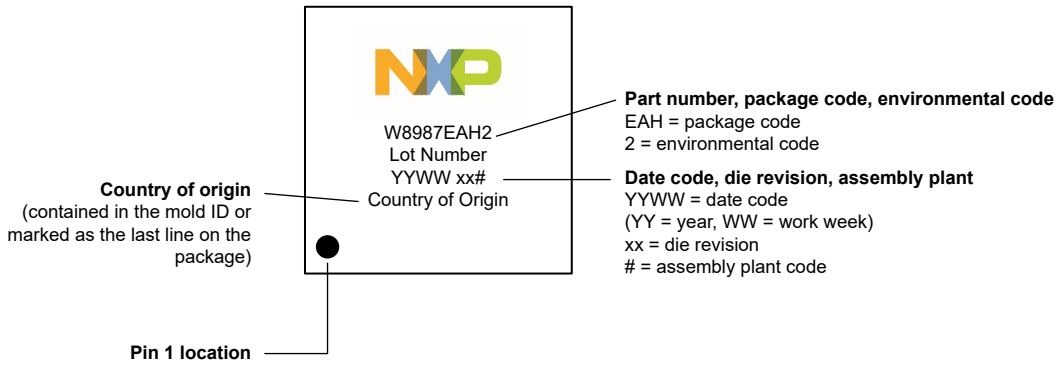
10.3.1 68-pin QFN package marking



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 29. 68-pin QFN package marking and pin 1 location

10.3.2 83-bump eWLP package marking



Note: The above drawing is not drawn to scale. The location of markings is approximate.

Figure 30. eWLP package marking and pin 1 location

11 Acronyms and abbreviations

Table 57. Acronyms and abbreviations

Acronym	Definition
A2DP	Advanced Audio Distribution Profiles
ABR	Automatic Baud Rate
ACK	Acknowledgment
ADAS	Advanced Driver Assistance Systems
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Correction
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIFS	Arbitration Interframe Space
AoA	Angle of Arrival
AoD	Angle of Departure
AP	Access Point
APB	Advanced Peripheral Bus
API	Application Program Interface
aQFN	Advanced Quad Flat Non-leaded Package
ARM	Advanced RISC Machine
ATIM	Announcement Traffic Indication Message
BAMR	Base Address Mask Register
BAR	Base Address Register
BBU	Baseband Processor Unit
BCB	Benzocyclobutene (flip chip bump process)
BDR	Basic Data Rate
BER	Bit Error Rate
BOM	Bill of Materials
BR	Baud Rate
BSS	Basic Service Set
BSSID	Basic Service Set Identifier
BTM	BSS Transition Management
BTU	Bluetooth Baseband Unit
BRF	Bluetooth RF Unit
BWQ	Bandwidth Queue
CBC	Cipher Block Chaining
CBP	Contention-Based Period

Table 57. Acronyms and abbreviations...*continued*

Acronym	Definition
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCMP	Counter Mode CBC-MAC Protocol
CDE	Close Descriptor Enable
CFP	Contention-Free Period
CFQ	Contention-Free Queue
CID	Connection Identifier
CIS	Card Information Structure
CIU	CPU Interface Unit
CMD	Command
CMQ	Control Management Queue
CRC	Cyclic Redundancy Check
CS	Card Select
CSL	Coordinated Sampled Listening
CSMA/CA	Carrier Sense Multiple Access / Collision Avoidance
CSMA/CD	Carrier Sense Multiple Access / Collision Detection
CSU	Clocked Serial Unit
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCD	Device Controller Driver
DCE	Data Communication Equipment
DCF	Distributed Coordination Function
DCLA	Direct Current Level Adjustment
DCLB	Digital Contactless Bridge
DCU	DMA Controller Unit
DFS	Dynamic Frequency Selection
DIFS	Distributed Interframe Space
DMA	Direct Memory Access
dQH	Device Queue Head
DQPSK	Differential Quadrature Phase Shift Keying
DSM	Distribution System Medium
DSP	Digital Signal Processor
DSRC	Dedicated Short Range Communications
dTD	Linked List Transfer Descriptors
DTIM	Delivery Traffic Indication Message

Table 57. Acronyms and abbreviations...*continued*

Acronym	Definition
DVSC	Digital Voltage Scaling Control
EAP	Extensible Authentication Protocol
EBRAM	Extended Block Random Access Memory
ED	Energy Detect
EDCA	Enhanced Distributed Channel Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EIFS	Extended Interframe Space
EMC	Electromagnetic Compatibility
ERP-OFDM	Extended Rate PHY-Orthogonal Frequency Division Multiplexing
ETSI	European Telecommunications Standards Institute
eWLP	Embedded Wafer Level Package
FAE	Field Application Engineer
FCC	Federal Communications Commission
FIFO	First In First Out
FIPS	Federal Information Processing Standards
FIQ	Fast Interrupt Request
FW	Firmware
GATT	Generic Attribute Profile
GCMP	Galois/Counter Mode Protocol
GI	Guard Interval
GPIO	General Purpose Input/Output
GPL	General Public License
GPU	General Purpose Input/Output Unit
HID	Human Interface Device
HIU	Host Interface Unit
HOGP	HID Over GATT Profile
HSP	Hands-Free Profile
HT	High Throughput
HW	Hardware
I/Q	Inphase/Quadrature
IB	InBand
IBSS	Independent Basic Service Set
ICE	In-Circuit Emulator (or Emulation)
ICR	Interrupt Cause Register
ICU	Interrupt Controller Unit
ICV	Integrity Check Value

Table 57. Acronyms and abbreviations*...continued*

Acronym	Definition
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers
IEMR	Interrupt Event Mask Register
I/F	Interface
IFS	Interframe Space
IMR	Interrupt Mask Register
IPG	Inter-Packet Gap
IPsec	Internet Protocol Security
IR	Infrared
IRQ	Interrupt Request
ISA	Instruction Set Architecture
ISDN	Integrated Services Digital Network
ISM	Industrial, Scientific, and Medical
ISMR	Interrupt Status Mask Register
ISR	Interrupt Status Register
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
LDPC	Low Density Parity Check
LE	Low Energy
LED	Light Emitting Diode
LME	Layer Management Entity
LNA	Low Noise Amplifier
LPM	Low Power Management
LQFN	Low Quad Flat Non-leaded
LSb	Least Significant bit
LSB	Least Significant Byte
LSP	Low-Speed Peripheral
LTE	Long Term Evolution
MAC	Media/Medium Access Controller
MC	Memory Controller
MCS	Modulation and Coding Scheme
MCU	MAC Control Unit
MDI	Modem Data Interface
MIB	Management Information Base
MIC	Message Integrity Code
MII	Media Independent Interface

Table 57. Acronyms and abbreviations*...continued*

Acronym	Definition
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions Per Second
MLME	MAC Sublayer Management Entity
MMI	Modem Management Interface
MMPDU	MAC Management Protocol Data Unit
MMU	Memory Management Unit
MPDU	MAC Protocol Data Unit
MSb	Most Significant bit
MSB	Most Significant Byte
MSDU	MAC Service Data Unit
MU-MIMO	Multi-User MIMO
MU-PPDU	Multi-User PPDU
MWS	Mobile Wireless System Multimedia Wireless System
NAV	Network Allocation Vector
NBS	Narrow band speech
NDP	Null Data Packet
NL	No Load
NPTR	Next Descriptor Pointer
Nsts	Number of space time streams
OCB	Outside the Context of a BSS
OFDM	Orthogonal Frequency Division Multiplexing
OID	Object Identifier
OOB	Out of Band
OTP	One Time Programmable
P2P	Peer-to-Peer
PA	Power Amplifier
PAD	Packet Assembler/Disassembler
PBU	Peripheral Bus Unit
PC	Point Coordinator
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCM	Pulse Code Modulation
PDn	Power Down

Table 57. Acronyms and abbreviations*...continued*

Acronym	Definition
PDU	Protocol Data Unit
PEAP	Protected EAP
PHY	Physical Layer
PIFS	Priority Interframe Space
PLL	Phase-Locked Loop
PLME	Physical Layer Management Entity
PMU	Power Management Unit
POST	Power-On Self Test
PPDU	PHY Protocol Data Unit
PPK	Per-Packet Key
PPM	Pulse Position Modulation
PSK	Pre-Shared Keys
PTA	Packet Traffic Arbitration
PWK	Pairwise Key
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non-leaded Package
QoS	Quality of Service
RA	Receiver Address
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RFID	Radio Frequency Identification
RIFS	Reduced Interframe Space
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSSI	Receiver Signal Strength Indication
RTS	Request to Send
RTU	General Purpose Timer Unit
RU	Resource Unit
SA	Source Address
SAP	Service Access Point
SCLK	Serial Interface Clock
SDA	Serial Interface Data
SE	Secure Element
SFD	Start of Frame Delimiter
SIFS	Short Interframe Space

Table 57. Acronyms and abbreviations...*continued*

Acronym	Definition
SISO	Single Input Single Output
SIU	Serial Interface Unit (UART)
SJU	System/Software JTAG Controller Unit
SM	Switch Module
SMI	Serial Management Interface
SNR	Signal-to-Noise Ratio
SO	Serial Out
SoC	System-on-Chip
SPDT	Single Pole Double Throw
SPI	Serial Peripheral Interface
SQU	Internal SRAM Unit
SRWB	Serial Interface Read Write
SS	Service Set
SSID	Service Set Identifier
STA	Station
STBC	Space-Time Block Code
SWD	Serial Wire Debug
SWP	Single Wire Protocol
TA	Transmitter Address
TBG	Time Base Generator
TBTT	Target Beacon Transmission Time
TCM	Tightly Coupled Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TCQ	Traffic Category Queue
TIM	Traffic Indication Map
TKIP	Temporal Key Integrity Protocol
TPC	Transmit Power Control
TQFP	Thin Quad Flat Pack
TRPC	Transmit Rate-based Power Control
TSC	TKIP Sequence Counter
TSF	Timing Synchronization Function
TWT	Target Wait Time
UART	Universal Asynchronous Receiver/Transmitter
UBM	Under Bump Metal
UDP	User Datagram Protocol
UNII	Unlicensed National Information Infrastructure

Table 57. Acronyms and abbreviations...*continued*

Acronym	Definition
VCO	Voltage Controlled Oscillator
VIF	Voice Interface
VHT	Very High Throughput
WAP	Wireless Application Protocol
WAVE	Wireless Access in Vehicular Environments
WBS	Wide band speech
WCI-2	Wireless Coexistence Interface 2
WEP	Wired Equivalent Privacy
WI	Wired Interface
Wi-Fi	Hardware implementation of IEEE 802.11 for wireless connectivity
WLAN	Wireless Local Area Network
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPA2	Wi-Fi Protected Access 2
WPA2-PSK	Wi-Fi Protected Access 2-Pre-Shared Key
WPA3	Wi-Fi Protected Access 3
WPA-PSK	Wi-Fi Protect Access-Pre-Shared Key
XFQFN	Extra-Fine Quad Flat Non-leaded
XOSC	Crystal Oscillator

12 Revision history

Table 58. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
88W8987 v.1.0	20201008	Product short data sheet	-	-

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Contents

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