SNx5176B 差动总线收发器

1 特性

- 双向收发器
- 符合或超出 ANSI 标准 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.11 和 X.27 的要求
- 适用于嘈杂环境中长距离总线线路上的多点传输
- 三态驱动器和接收器输出
- 单独的驱动器和接收器使能端
- 宽正负输入/输出总线电压范围
- ±60mA 最大驱动器输出能力
- 热关断保护
- 驱动器正负电流限制
- 12kΩ 最小接收器输入阻抗
- ±200mV 接收器输入灵敏度
- 50mV 典型接收器输入迟滞
- 由 5V 单电源供电

2 应用

- 化学和气体传感器
- 数字标牌
- HMI（人机界面）
- 电机控制：交流感应、刷式和无刷直流、低电压和高电压、步进电机和永磁体
- TETRA 基站
- 电信塔：远程电动倾斜单元 (RET) 和塔顶放大器 (TMA)
- 称重秤
- 无线中继器

3 说明

SN65176B 和 SN75176B 差分总线收发器旨在实现多点总线传输线路上的双向数据通信。这些器件专为平衡传输线路而设计，符合 ANSI 标准 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.11 和 X.27。

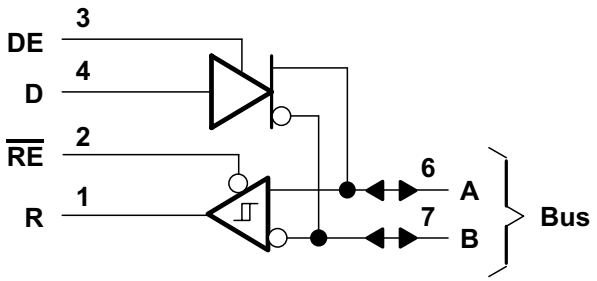
SN65176B 和 SN75176B 器件整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，这些端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。这些端口具有较宽的正负共模电压范围，使得该器件适用于合用线应用。

驱动器旨在实现高达 60mA 的灌电流或拉电流。驱动器具有正负电流限制和热关断功能，避免出现线路故障状况。根据设计在大约 150°C 的结温下发生热关断。接收器具有 12kΩ 的最小输入阻抗、±200mV 的输入灵敏度和 50mV 的典型输入迟滞。

器件信息

器件型号	封装（引脚）(1)	封装尺寸（标称值）
SNx5176	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm
	SOP (8)	6.20mm × 5.30mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

Changes from Revision G (July 2021) to Revision H (December 2021) **Page**

- Changed ψ_{JT} From 78.8 to 8.8 for the D package in the *Thermal Information* table.....4

Changes from Revision F (January 2015) to Revision G (July 2021) **Page**

- Changed the *Thermal Information* table.....4
- Changed the V_O Output voltage MAX value from: 6 V to: V_{CC} in the *Electrical Characteristics – Driver*.....5
- Changed the V_{ODI} Differential output voltage MAX value from: 6 V to: V_{CC} in the *Electrical Characteristics – Driver*.....5

Changes from Revision E (January 2014) to Revision F (January 2015) **Page**

- 添加了*应用*、*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分.....1
- Moved *Typical Characteristics* inside of the *Specifications* section.....7

Changes from Revision D (April 2003) to Revision E (January 2014) **Page**

- 将文档更新为新的 TI 数据表格式 - 无规格变化.....1
- 删除了*订购信息* 表.....1

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5 Pin Configuration and Functions

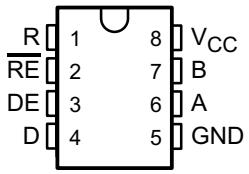

图 5-1. Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Logic Data Output from RS-485 Receiver
$\overline{RE}$	2	I	Receive Enable (active low)
DE	3	I	Driver Enable (active high)
D	4	I	Logic Data Input to RS-485 Driver
GND	5	—	Device Ground Pin
A	6	I/O	RS-422 or RS-485 Data Line
B	7	I/O	RS-422 or RS-485 Data Line
V_{CC}	8	—	Power Input. Connect to 5-V Power Source.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		-7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65176B	–40		105	°C
		SN75176B	0		70	

(1) Differential input/output bus voltage is measured at the non-inverting terminal A, with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC(1)		SNx5176			UNIT
		D (SOIC)	PS (SO)	P (PDIP)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.4	113.2	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	57.9	65.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.6	69.0	69.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	14.6	35.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	68.1	64.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

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6.4 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		Vcc	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	Vcc	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, see 图 7-1		½ V_{OD1} or 2 (4)			V
		R_L = 54 Ω, see 图 7-1		1.5	2.5	5	
V_{OD3}	Differential output voltage	See (5)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	R_L = 54 Ω or 100 Ω, see 图 7-1				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω, see 图 7-1		-1		+3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)	R_L = 54 Ω or 100 Ω, see 图 7-1				±0.2	V
I_O	Output current	Output disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

(1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) The minimum V_{OD2} with a 100-Ω load is either ½ V_{OD1} or 2 V, whichever is greater.
(5) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
(6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

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6.5 Electrical Characteristics – Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V, I_O = 8 mA		–0.2(2)			V
V_{hys}	Input hysteresis voltage (V_{IT+} – V_{IT-})				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –400 µA, see 图 7-2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, see 图 7-2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

6.6 Switching Characteristics – Driver

V_{CC} = 5 V, R_L = 110 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, see 图 7-3		15	22	ns
$t_{t(OD)}$	Differential-output transition time	R_L = 54 Ω, see 图 7-3		20	30	ns
t_{PZH}	Output enable time to high level	See 图 7-4		85	120	ns
t_{PZL}	Output enable time to low level	See 图 7-5		40	60	ns
t_{PHZ}	Output disable time from high level	See 图 7-4		150	250	ns
t_{PLZ}	Output disable time from low level	See 图 7-5		20	30	ns

6.7 Switching Characteristics – Receiver

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, see 图 7-6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level	See 图 7-7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level	See 图 7-7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

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6.8 Typical Characteristics

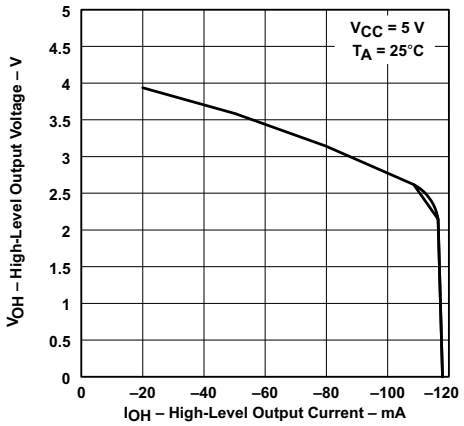


图 6-1. Driver High-Level Output Voltage vs High-Level Output Current

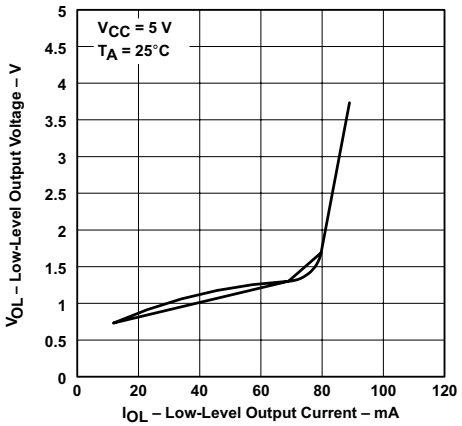


图 6-2. Driver Low-Level Output Voltage vs Low-Level Output Current

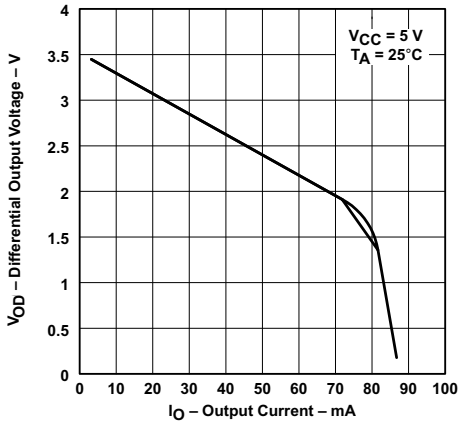


图 6-3. Driver Differential Output Voltage vs Output Current

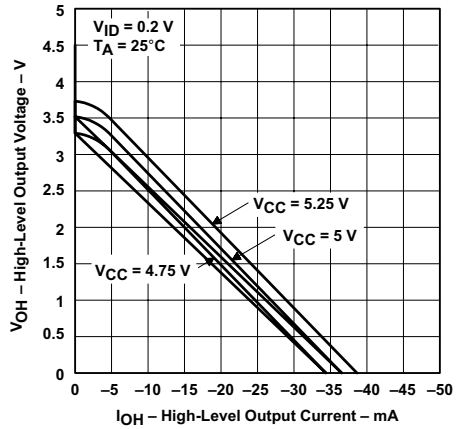
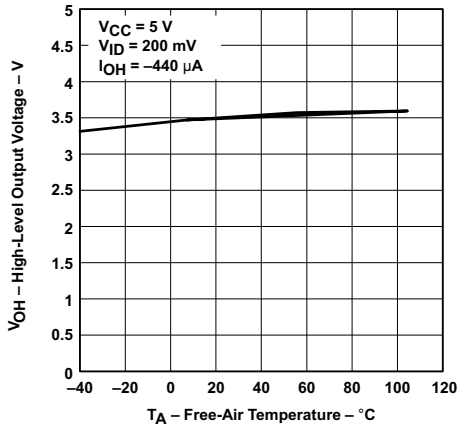


图 6-4. Receiver High-Level Output Voltage vs High-Level Output Current



Only the 0°C to 70°C portion of the curve applies to the SN75176B device.

图 6-5. Receiver High-Level Output Voltage vs Free-Air Temperature

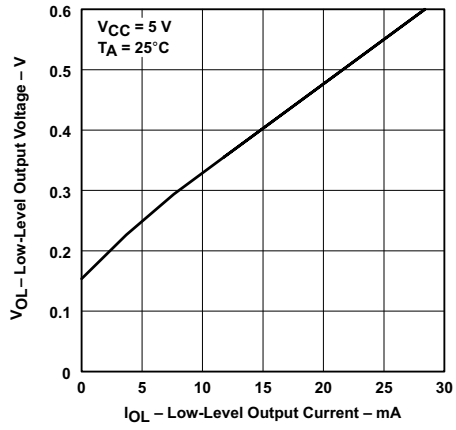


图 6-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

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6.8 Typical Characteristics (continued)

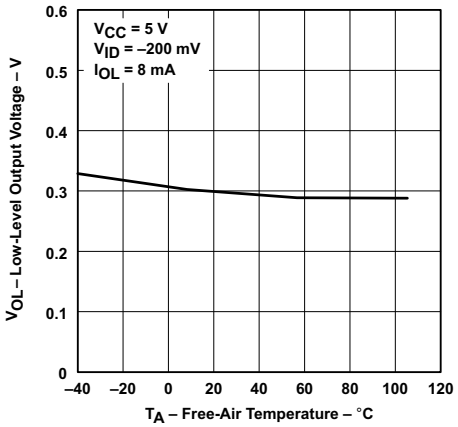

图 6-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

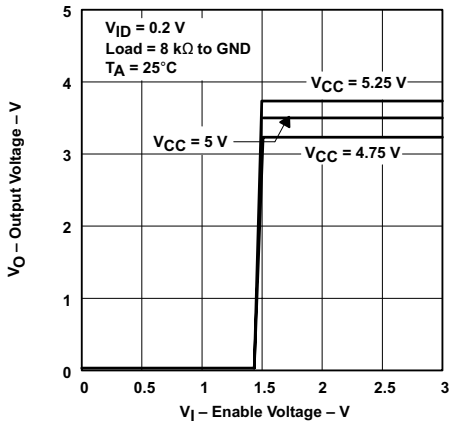

图 6-8. Receiver Output Voltage vs Enable Voltage

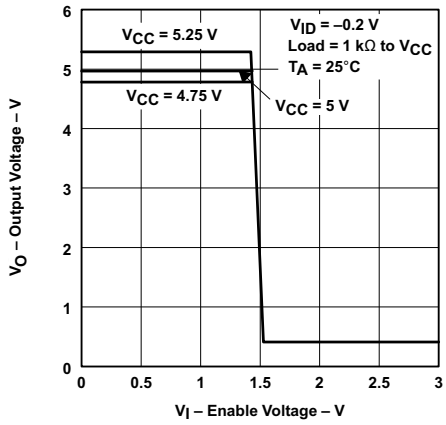

图 6-9. Receiver Output Voltage vs Enable Voltage

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Parameter Measurement Information

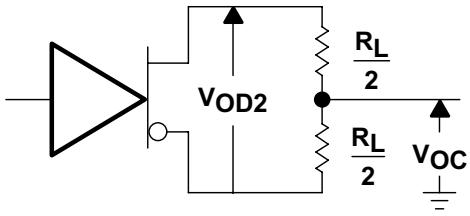


图 7-1. Driver V_{OD} and V_{OC}

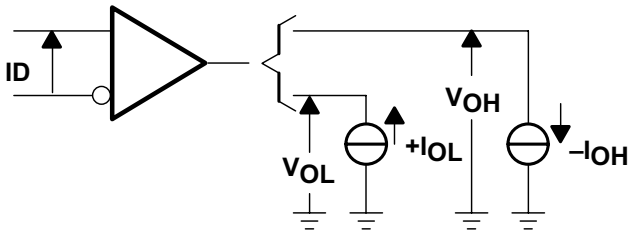
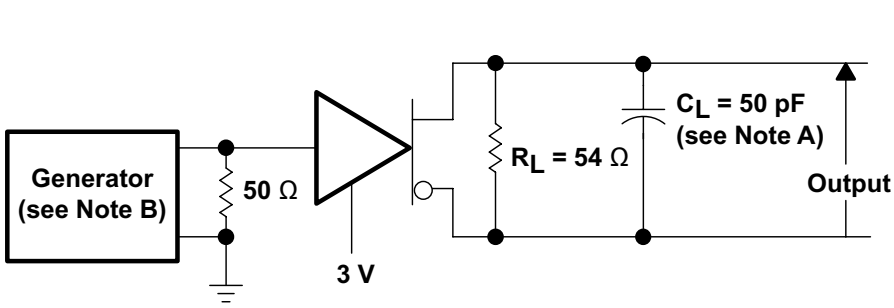
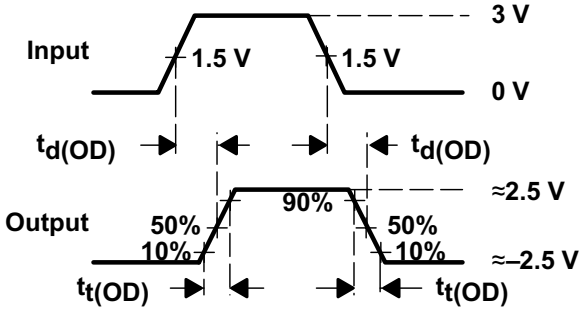


图 7-2. Receiver V_{OH} and V_{OL}



TEST CIRCUIT

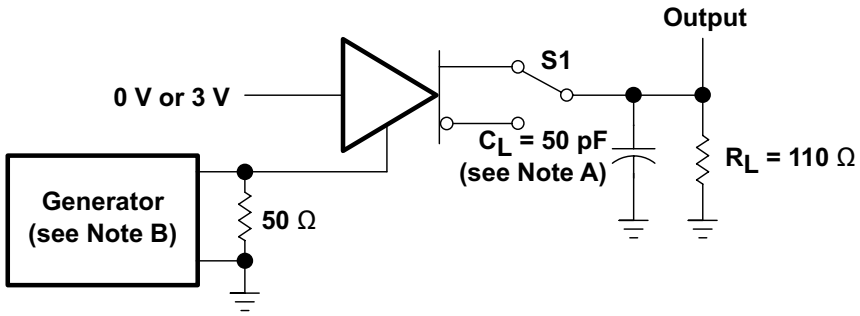


VOLTAGE WAVEFORMS

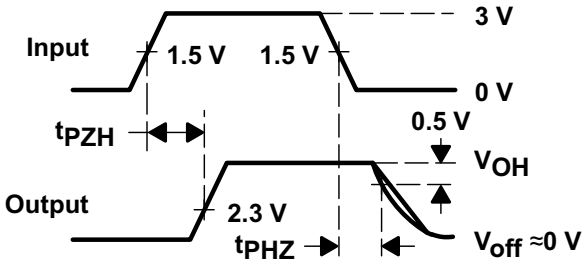
A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

图 7-3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

图 7-4. Driver Test Circuit and Voltage Waveforms

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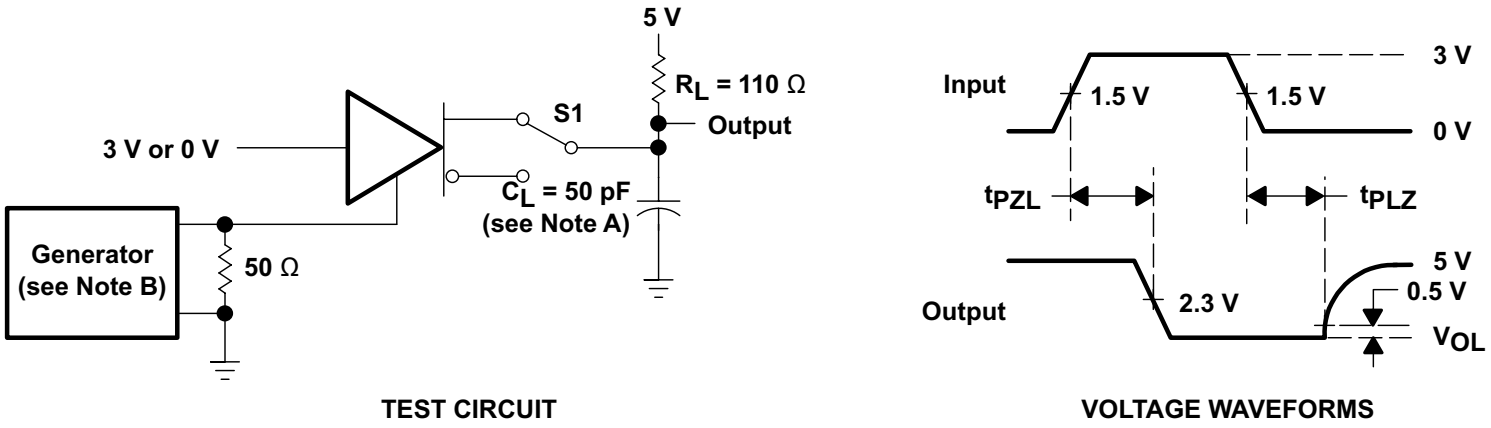
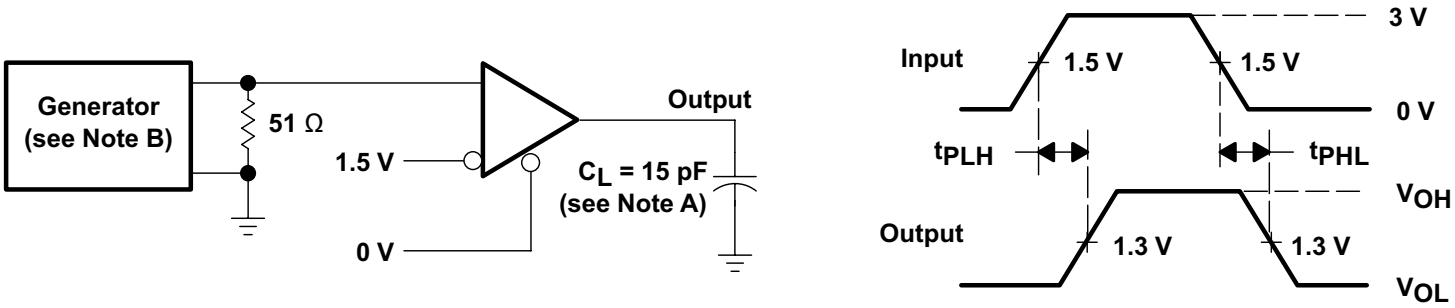


A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

图 7-5. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

图 7-6. Receiver Test Circuit and Voltage Waveforms

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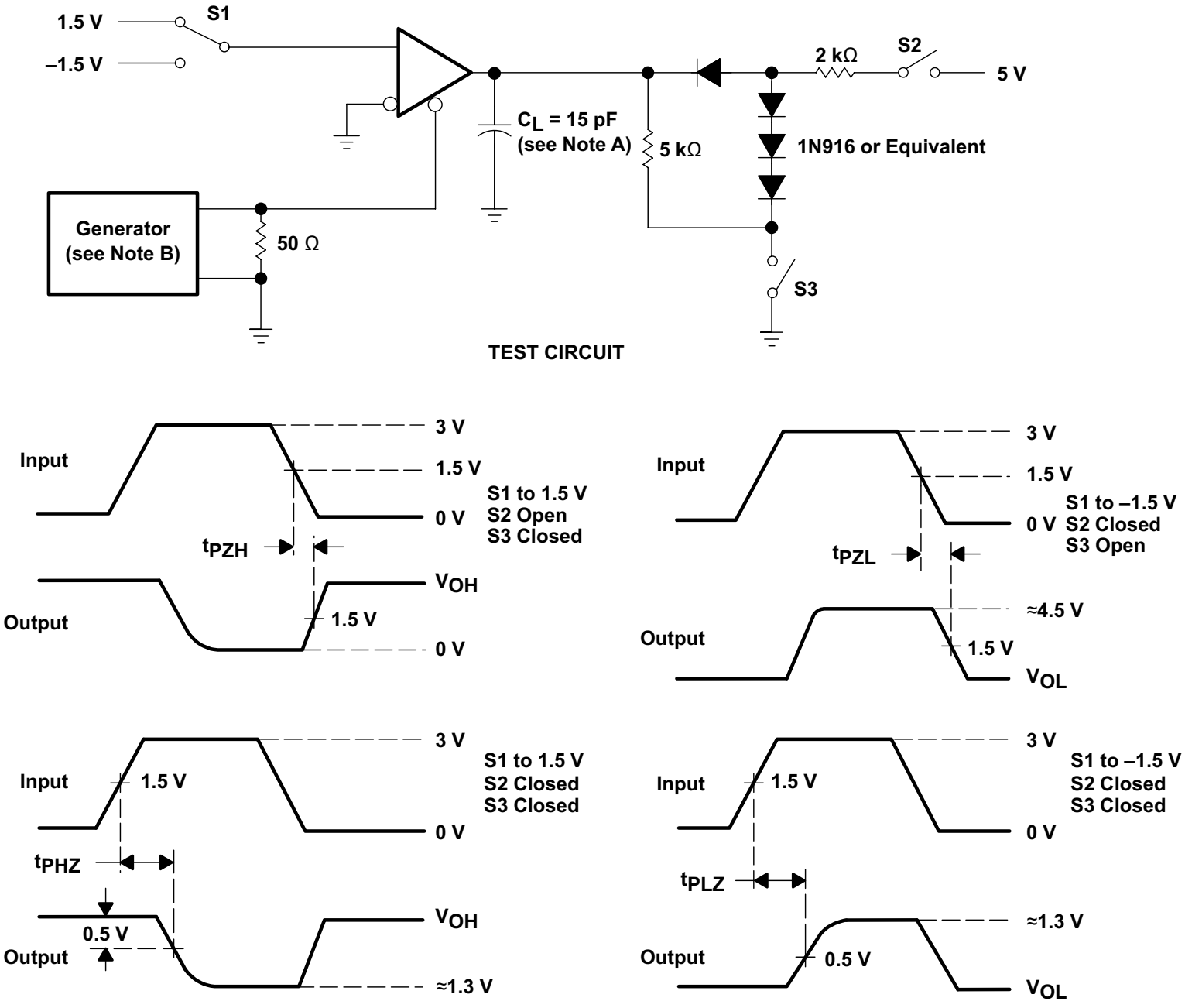

A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ⩽1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

图 7-7. Receiver Test Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

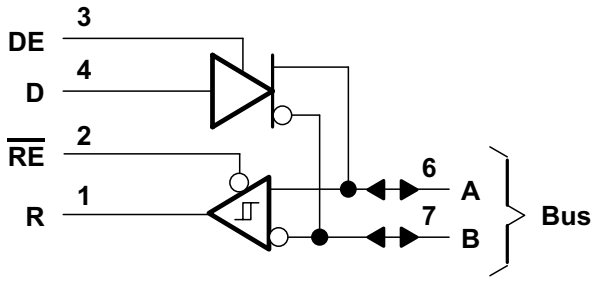
The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B devices can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. The TTL logic input, DE pin, can be used to turn the driver on and off.

表 7-1. Driver Function Table(1)

INPUT D	ENABLE DE	DIFFERENTIAL OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

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7.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. The TTL logic input, $\overline{RE}$ pin, can be used to turn the receiver logic output on and off.

表 7-2. Receiver Function Table(1)

DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
– 0.2 V < V_{ID} < 0.2 V	L	U
$V_{ID} \leq$ – 0.2 V	L	L
X	H	Z
Open	L	U

(1) H = high level,
L = low level,
U = unknown,
Z = high impedance (off)

7.4 Device Functional Modes

7.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and $\overline{RE}$ can be connected together for a single port direction control bit.

7.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

7.4.3 Symbol Cross Reference

表 7-3. Symbol Equivalents

DATA SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t ®$_L$ = 100 Ω)	V_t ®$_L$ = 54 Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\|\|V_t\| - \|\overline{V}_t\|\|$	$\|\|V_t - \|\overline{V}_t\|\|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

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8 Application and Implementation

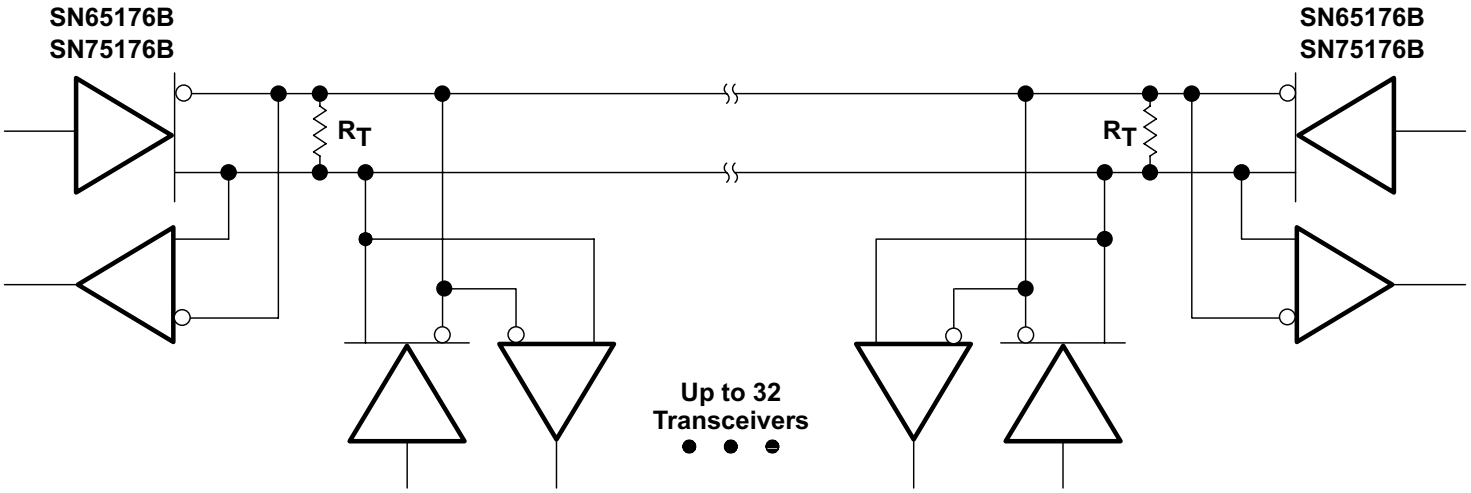
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The device can be used in RS-485 and RS-422 physical layer communications.

8.2 Typical Application



The line should be terminated at both ends in its characteristic impedance ®$_T$ = Z_O). Stub lengths off the main line should be kept as short as possible.

图 8-1. Typical RS-485 Application Circuit

8.2.1 Design Requirements

- 5-V power source
- RS-485 bus operating at 10 Mbps or less
- Connector that ensures the correct polarity for port pins
- External fail safe implementation

8.2.2 Detailed Design Procedure

- Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line
- If desired, add external fail-safe biasing to ensure +200 mV on the A-B port.

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8.2.3 Application Curves

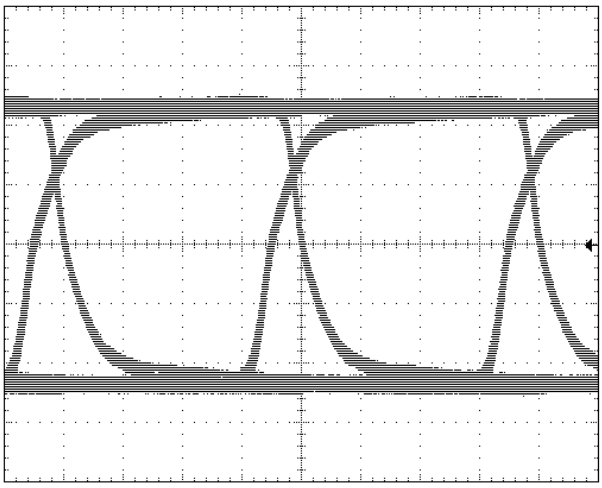

图 8-2. Eye Diagram for 10-Mbits/s over 100 feet of standard CAT-5E cable 120-Ω Termination at both ends. Scale is 1 V per division and 25 nS per division

8.3 System Examples

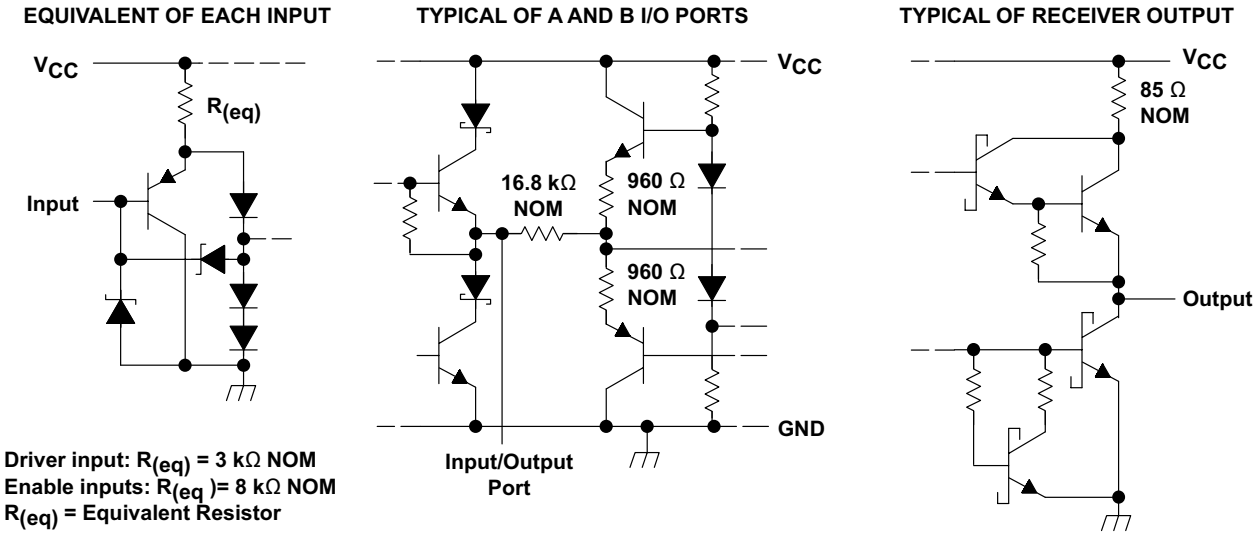

图 8-3. Schematics of Inputs and Outputs

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9 Power Supply Recommendations

Power supply should be 5 V with a tolerance less than 10%

10 Layout

10.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

10.2 Layout Example

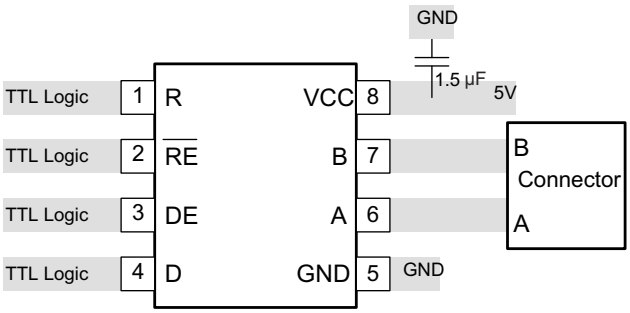

图 10-1. Layout Diagram

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11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65176B	Click here	Click here	Click here	Click here	Click here
SN75176B	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

所有商标均为其各自所有者的财产。

11.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65176BD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	
SN65176BDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	
SN65176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	SN65176BP	Samples
SN75176BD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDE4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75176BP	Samples
SN75176BPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75176BP	Samples
SN75176BPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B	Samples
SN75176BPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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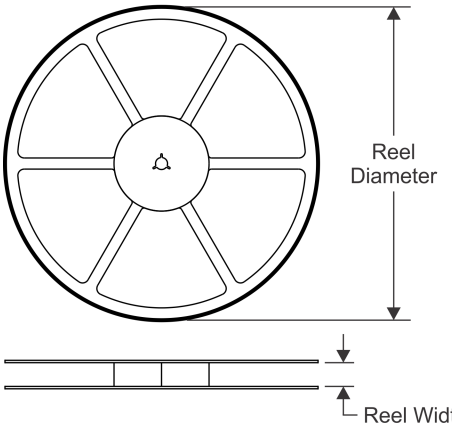
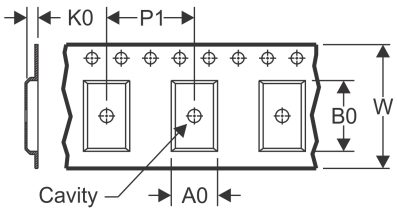
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

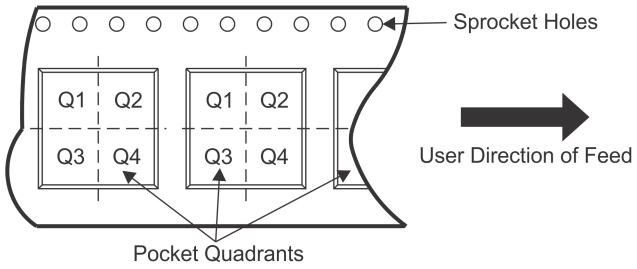


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

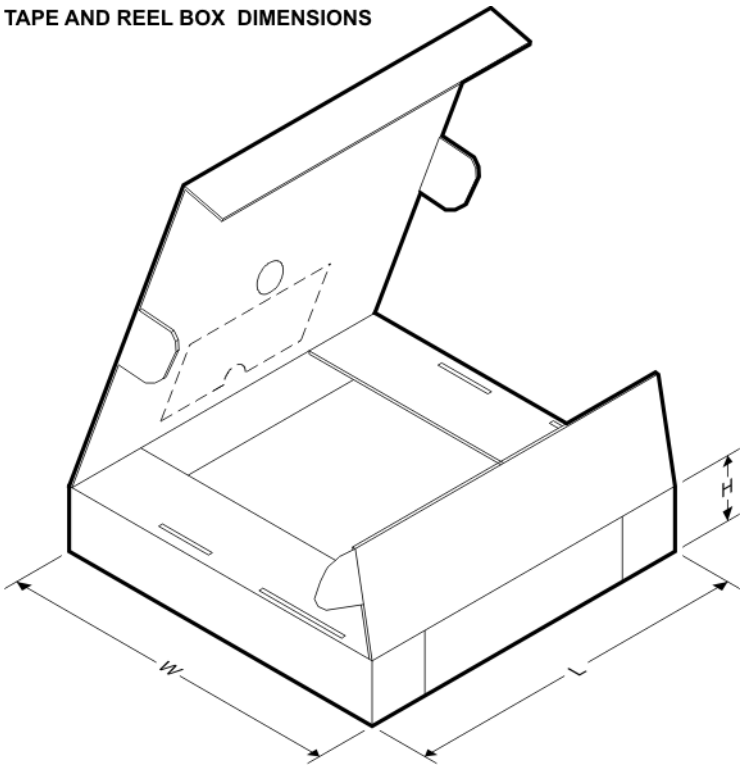
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75176BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

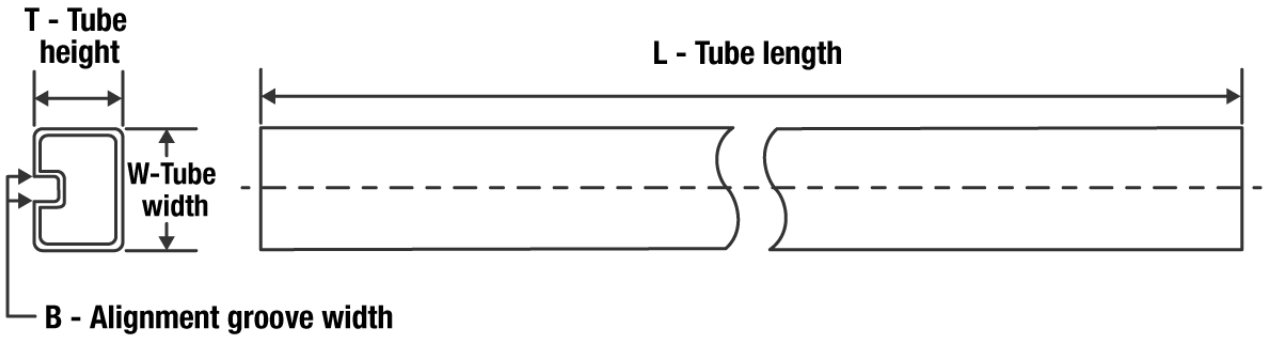
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

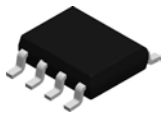
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65176BDR	SOIC	D	8	2500	367.0	367.0	35.0
SN65176BDR	SOIC	D	8	2500	340.5	336.1	25.0
SN65176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65176BDRG4	SOIC	D	8	2500	367.0	367.0	35.0
SN65176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75176BDR	SOIC	D	8	2500	367.0	367.0	35.0
SN75176BDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDRG4	SOIC	D	8	2500	367.0	367.0	35.0
SN75176BPSR	SO	PS	8	2000	853.0	449.0	35.0
SN75176BPSR	SO	PS	8	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65176BD	D	SOIC	8	75	507	8	3940	4.32
SN65176BDG4	D	SOIC	8	75	507	8	3940	4.32
SN65176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BD	D	SOIC	8	75	507	8	3940	4.32
SN75176BDE4	D	SOIC	8	75	507	8	3940	4.32
SN75176BDG4	D	SOIC	8	75	507	8	3940	4.32
SN75176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BPE4	P	PDIP	8	50	506	13.97	11230	4.32

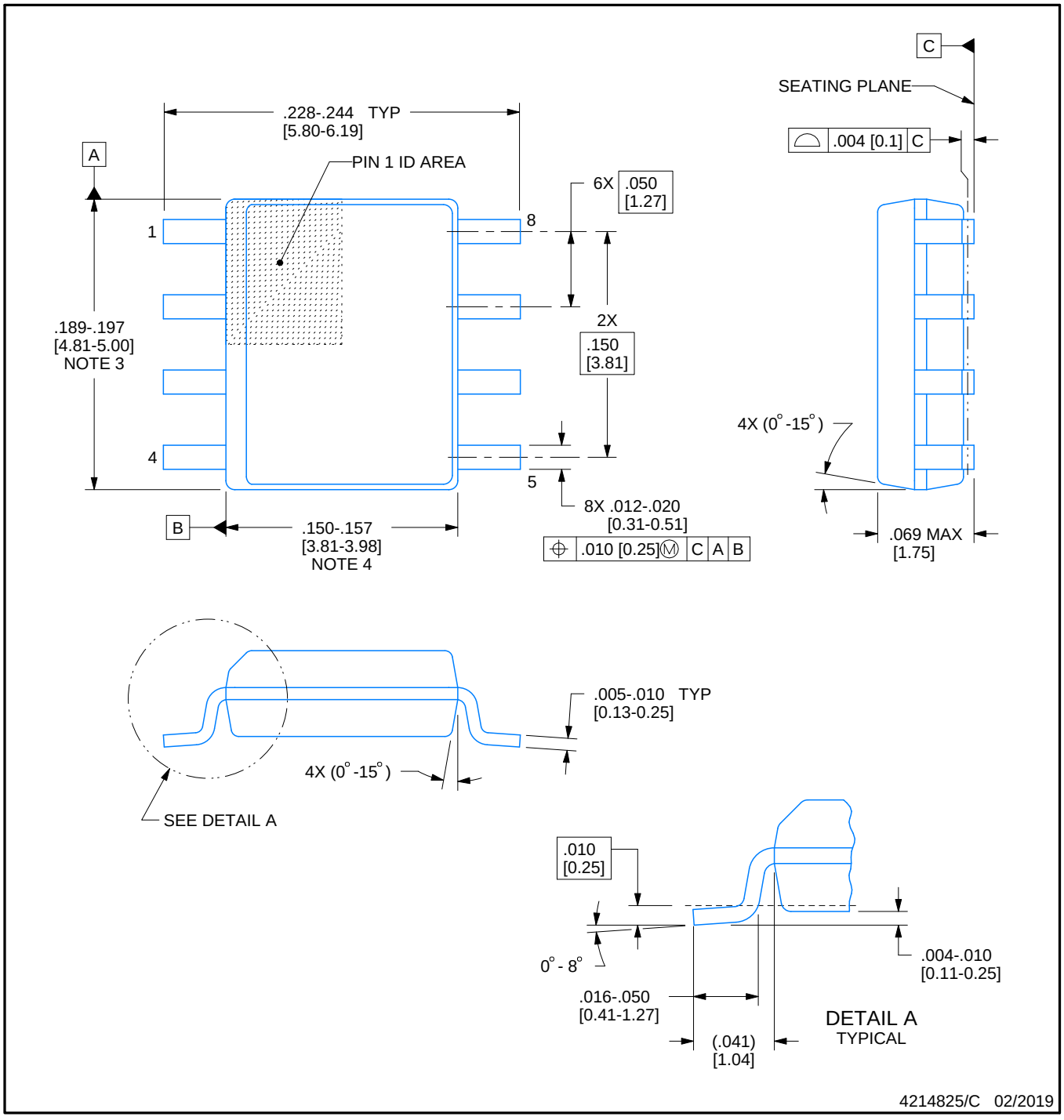


PACKAGE OUTLINE

D0008A

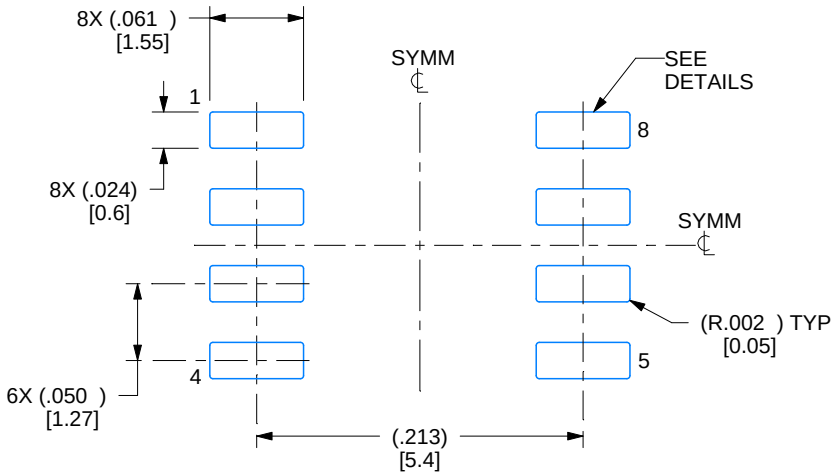
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

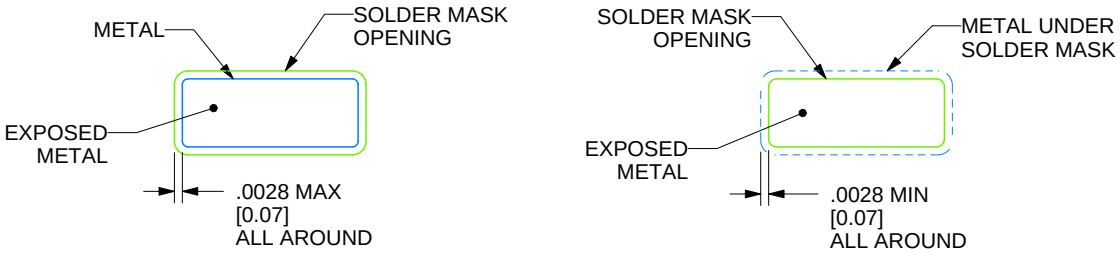


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

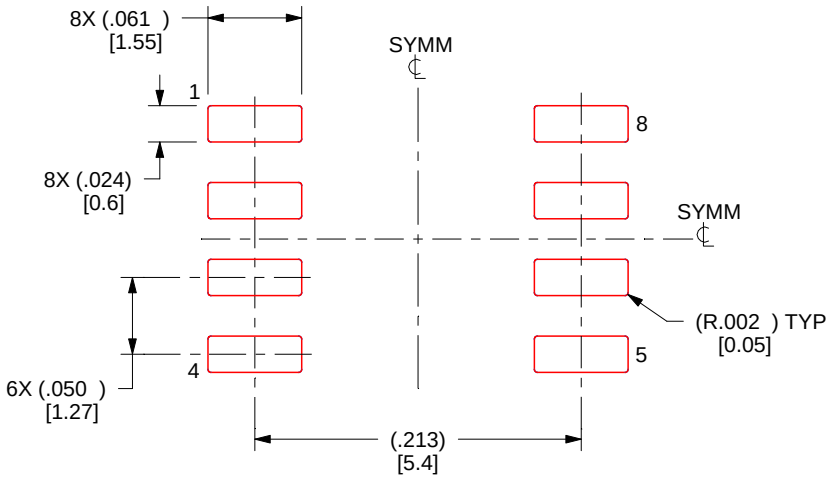
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

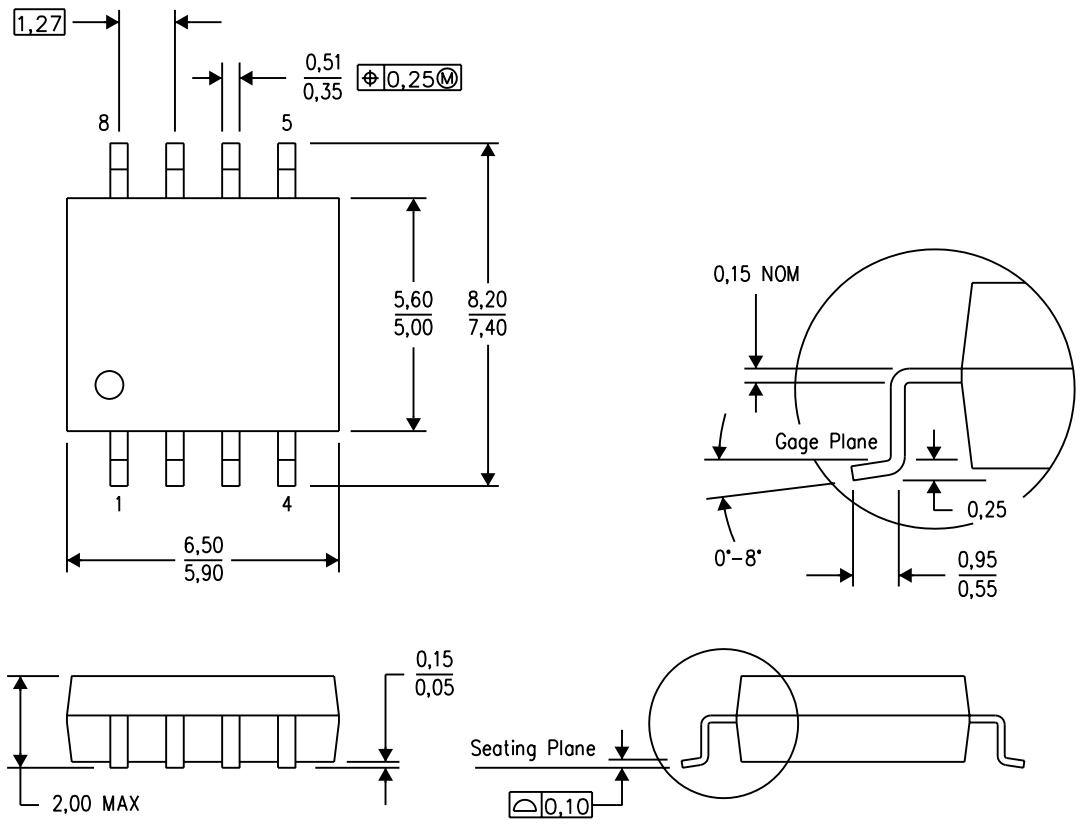
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

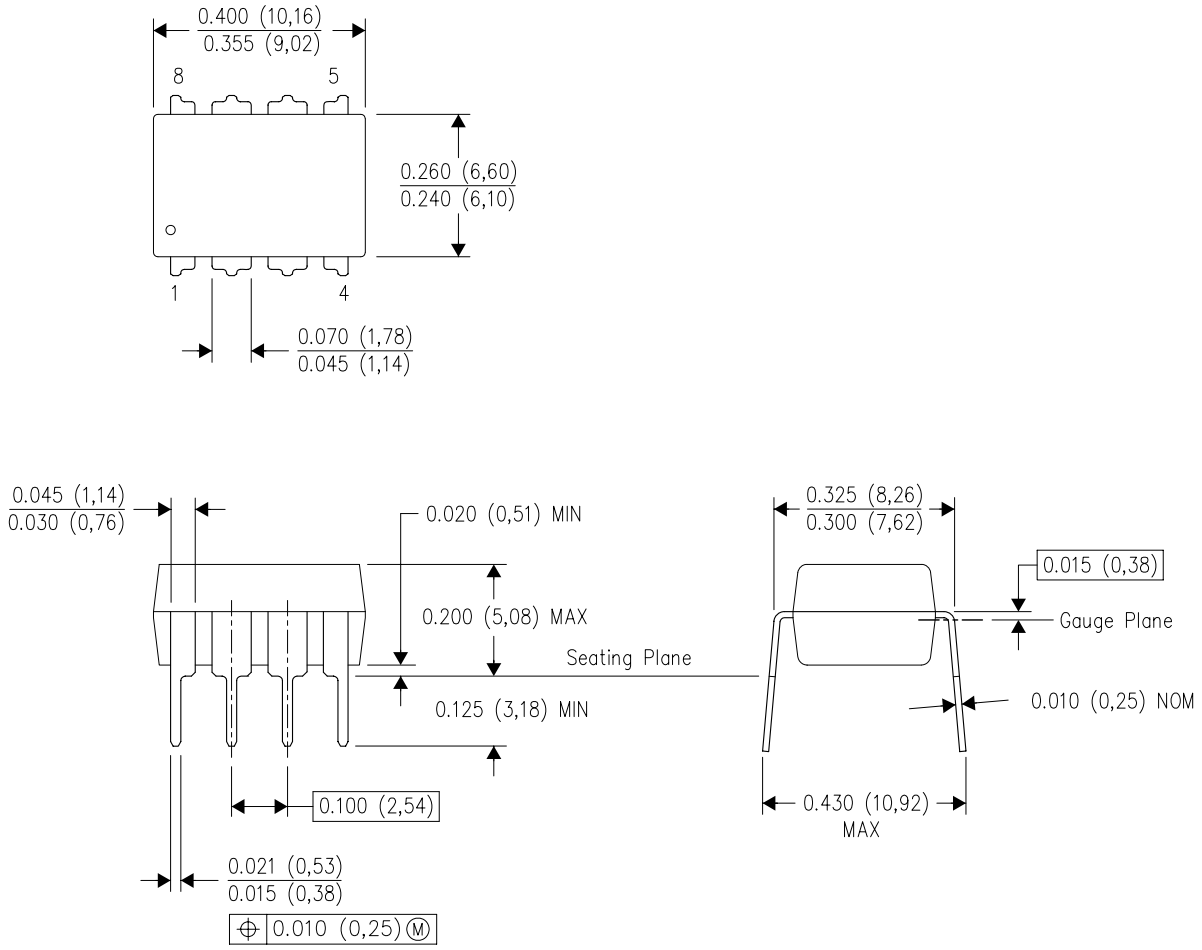
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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