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Jameco Part Number 914398

# DATA SHEET

**74HCT9046A**

**PLL with band gap controlled VCO**

Product specification  
Supersedes data of 2003 May 15

2003 Oct 30

## PLL with band gap controlled VCO

## 74HCT9046A

### FEATURES

- Operation power supply voltage range from 4.5 to 5.5 V
- Low power consumption
- Inhibit control for ON/OFF keying and for low standby power consumption
- Centre frequency up to 17 MHz (typical) at  $V_{CC} = 5.5$  V
- Choice of two phase comparators:
  - PC1: EXCLUSIVE-OR
  - PC2: Edge-triggered JK flip-flop.
- No dead zone of PC2
- Charge pump output on PC2, whose current is set by an external resistor  $R_b$
- Centre frequency tolerance  $\pm 10\%$
- Excellent Voltage Controlled Oscillator (VCO) linearity
- Low frequency drift with supply voltage and temperature variations
- On-chip band gap reference
- Glitch free operation of VCO, even at very low frequencies
- Zero voltage offset due to op-amp buffering
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.

### APPLICATIONS

- FM modulation and demodulation where a small centre frequency tolerance is essential
- Frequency synthesis and multiplication where a low jitter is required (e.g. video picture-in-picture)
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

### GENERAL DESCRIPTION

The 74HCT9046A is a high-speed Si-gate CMOS device. It is specified in compliance with JEDEC standard no 7A.

### QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 6$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$f_c$	VCO centre frequency	$C_1 = 40$ pF; $R_1 = 3$ k $\Omega$ ; $V_{CC} = 5$ V	16	MHz
$C_I$	input capacitance		3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	20	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacitance in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total load switching outputs;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. Applies to the phase comparator section only (pin INH = HIGH). For power dissipation of the VCO and demodulator sections, see Figs 26 to 28.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PACKAGE	MATERIAL	CODE
74HCT9046AN	16	DIP16	plastic	SOT38-1
74HCT9046AD	16	SO16	plastic	SOT109-1
74HCT9046APW	16	TSSOP16	plastic	SOT403-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	GND	ground (0 V) of phase comparators
2	PC1_OUT/ PCP_OUT	phase comparator 1 output or phase comparator pulse output
3	COMP_IN	comparator input
4	VCO_OUT	VCO output
5	INH	inhibit input
6	C1A	capacitor C1 connection A
7	C1B	capacitor C1 connection B
8	GND	ground (0 V) VCO
9	VCO_IN	VCO input
10	DEM_OUT	demodulator output
11	R1	resistor R1 connection
12	R2	resistor R2 connection
13	PC2_OUT	phase comparator 2 output; current source adjustable with $R_b$
14	SIG_IN	signal input
15	RB	bias resistor ( $R_b$ ) connection
16	V <sub>CC</sub>	supply voltage

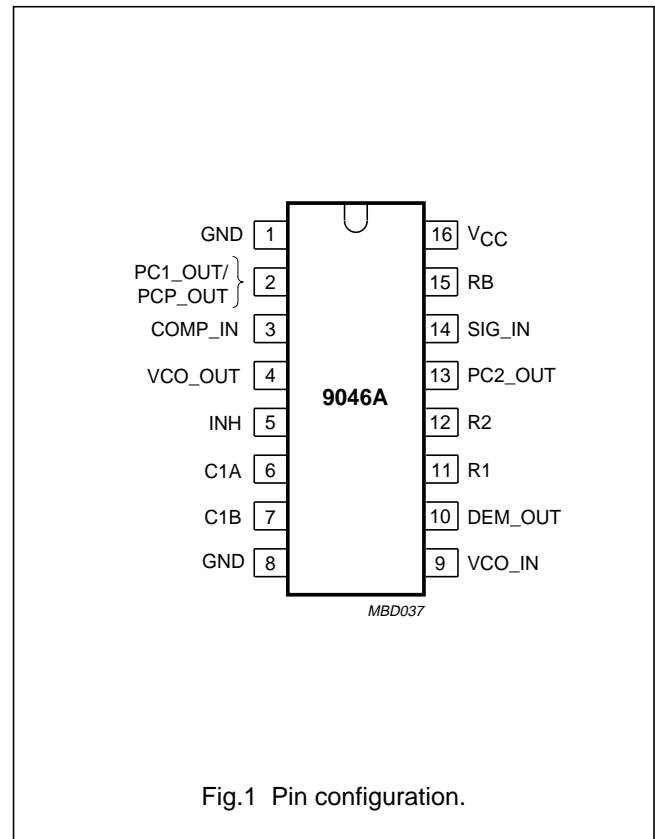
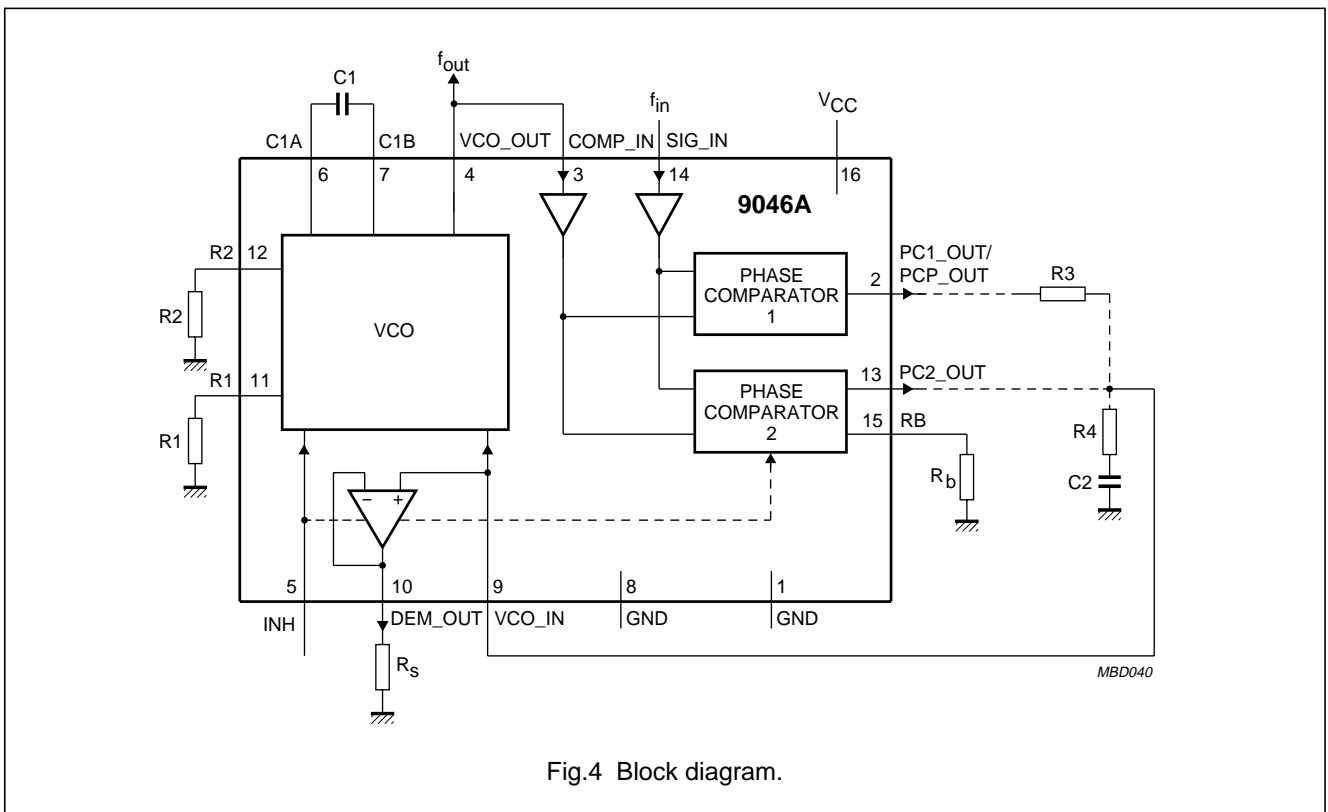
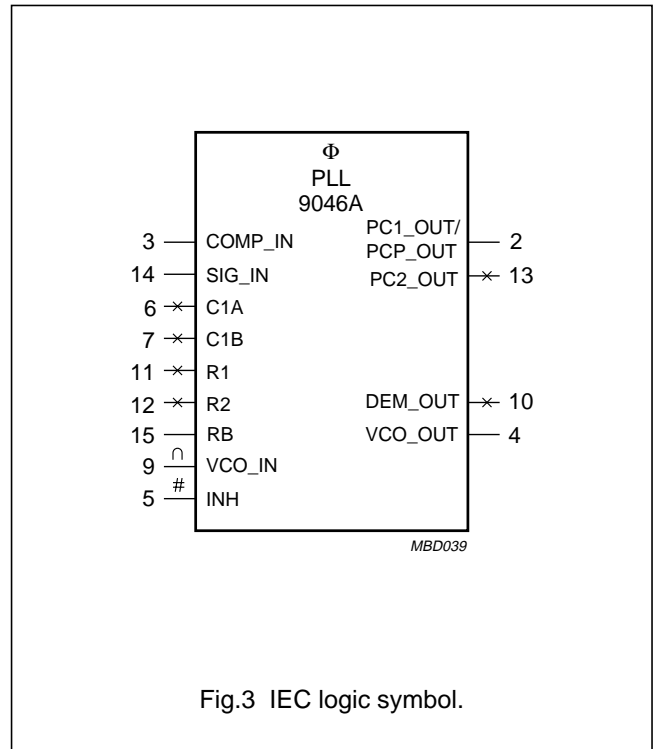
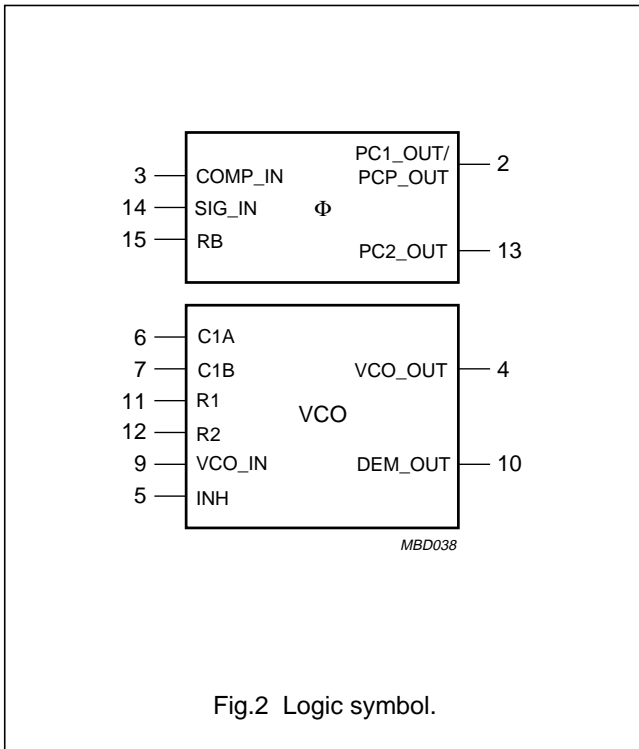


Fig.1 Pin configuration.

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LOGIC AND FUNCTIONAL SYMBOLS AND DIAGRAMS



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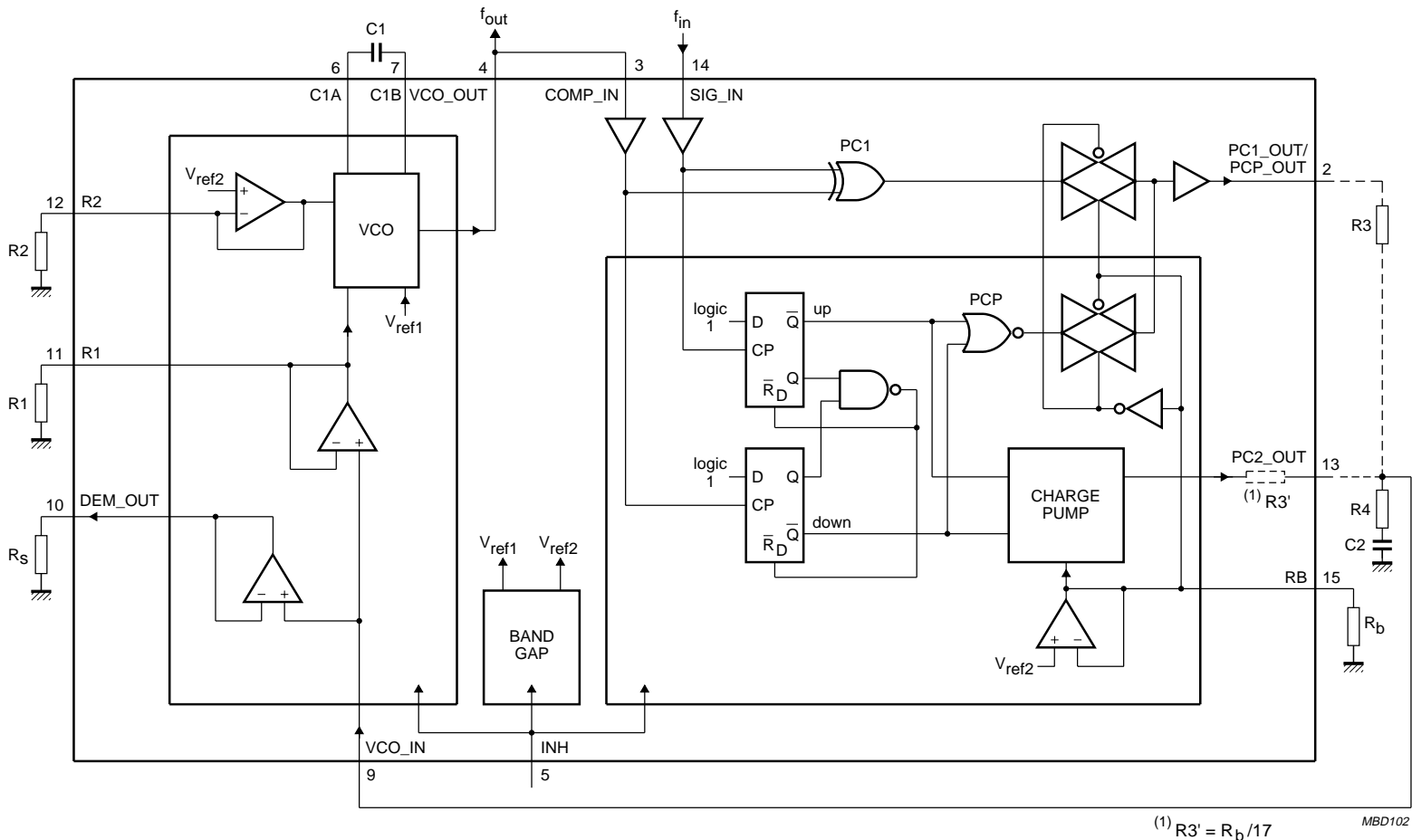


Fig.5 Logic diagram.

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### FUNCTIONAL DESCRIPTION

The 74HCT9046A is a phase-locked-loop circuit that comprises a linear VCO and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input (see Fig.4). The signal input can be directly coupled to large voltage signals (CMOS level), or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the 74HCT9046A forms a second-order loop PLL.

The principle of this phase-locked-loop is based on the familiar 74HCT4046A. However extra features are built-in, allowing very high-performance phase-locked-loop applications. This is done, at the expense of PC3, which is skipped in this 74HCT9046A. The PC2 is equipped with a current source output stage here. Further a band gap is applied for all internal references, allowing a small centre frequency tolerance. The details are summed up in the next section: "Differences with respect to the familiar 74HCT4046A". If one is familiar with the 74HCT4046A already, it will do to read this section only.

### Differences with respect to the familiar 74HCT4046A

- A centre frequency tolerance of maximum  $\pm 10\%$ .
  - The on board band gap sets the internal references resulting in a minimal frequency shift at supply voltage variations and temperature variations.
  - The value of the frequency offset is determined by an internal reference voltage of 2.5 V instead of  $V_{CC} - 0.7$  V. In this way the offset frequency will not shift over the supply voltage range.
  - A current switch charge pump output on pin PC2\_OUT allows a virtually ideal performance of PC2. The gain of PC2 is independent of the voltage across the low-pass filter. Further a passive low-pass filter in the loop achieves an active performance. The influence of the parasitic capacitance of the PC2 output plays no role here, resulting in a true correspondence of the output correction pulse and the phase difference even up to phase differences as small as a few nanoseconds.
  - Because of its linear performance without dead zone, higher impedance values for the filter, hence lower C-values, can now be chosen. Correct operation will not be influenced by parasitic capacitances as in the instance with voltage source output of the 4046A.
- No PC3 on pin RB but instead a resistor connected to GND, which sets the load/unload currents of the charge pump (PC2).
  - Extra GND pin 1 to allow an excellent FM demodulator performance even at 10 MHz and higher.
  - Combined function of pin PC1\_OUT/PCP\_OUT. If pin RB is connected to  $V_{CC}$  (no bias resistor  $R_b$ ) pin PC1\_OUT/PCP\_OUT has its familiar function viz. output of PC1. If at pin RB a resistor ( $R_b$ ) is connected to GND it is assumed that PC2 has been chosen as phase comparator. Connection of  $R_b$  is sensed by internal circuitry and this changes the function of pin PC1\_OUT/PCP\_OUT into a lock detect output (PCP\_OUT) with the same characteristics as PCP\_OUT of pin 1 of the 74HCT4046A.
  - The inhibit function differs. For the HCT4046A a HIGH level at the inhibit input (pin INH) disables the VCO and demodulator, while a LOW level turns both on. For the 74HCT9046A a HIGH level on the inhibit input disables the whole circuit to minimize standby power consumption.

### VCO

The VCO requires one external capacitor C1 (between pins C1A and C1B) and one external resistor R1 (between pins R1 and GND) or two external resistors R1 and R2 (between pins R1 and GND, and R2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required (see Fig.5).

The high input impedance of the VCO simplifies the design of the low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin DEM\_OUT. The DEM\_OUT voltage equals that of the VCO input. If DEM\_OUT is used, a load resistor ( $R_s$ ) should be connected from pin DEM\_OUT to GND; if unused, DEM\_OUT should be left open. The VCO output (pin VCO\_OUT) can be connected directly to the comparator input (pin COMP\_IN), or connected via a frequency divider. The output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (pin INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

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## Phase comparators

The signal input (pin SIG\_IN) can be directly coupled to the self-biasing amplifier at pin SIG\_IN, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

### PHASE COMPARATOR 1 (PC1)

This circuit is an EXCLUSIVE-OR network. The signal and comparator input frequencies ( $f_i$ ) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ( $f_r = 2f_i$ )

is suppressed, is:  $V_{DEM\_OUT} = \frac{V_{CC}}{\pi} (\Phi_{SIG\_IN} - \Phi_{COMP\_IN})$

where:

$V_{DEM\_OUT}$  is the demodulator output at pin DEM\_OUT.

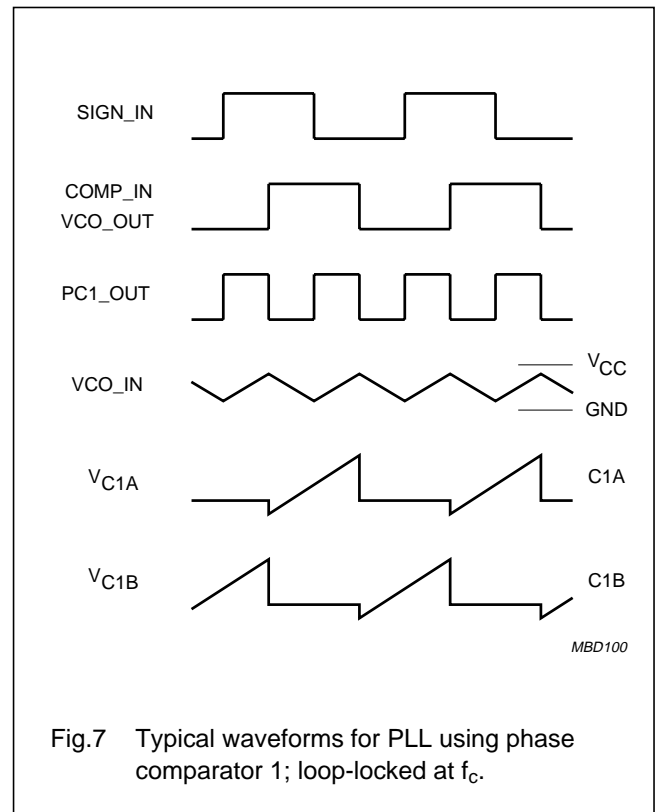
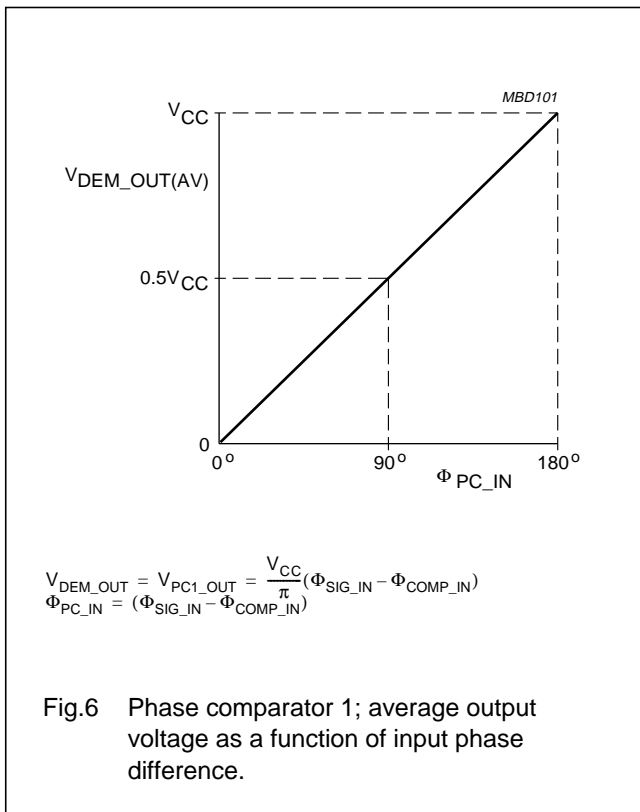
$V_{DEM\_OUT} = V_{PC1\_OUT}$  (via low-pass).

The phase comparator gain is:  $K_p = \frac{V_{CC}}{\pi} (V/r)$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin DEM\_OUT ( $V_{DEM\_OUT}$ ), is the resultant of the phase differences of signals (SIG\_IN) and the comparator input (COMP\_IN) as shown in Fig.6. The average of  $V_{DEM\_OUT}$  is equal to  $0.5V_{CC}$  when there is no signal or noise at SIG\_IN and with this input the VCO oscillates at the centre frequency ( $f_c$ ). Typical waveforms for the PC1 loop locked at  $f_c$  are shown in Fig.7. This figure also shows the actual waveforms across the VCO capacitor at pins C1A and C1B ( $V_{C1A}$  and  $V_{C1B}$ ) to show the relation between these ramps and the VCO\_OUT voltage.

The frequency capture range ( $2f_c$ ) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ( $2f_L$ ) is defined as the frequency range of the input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration remains locked even with very noisy input signals. Typical behaviour of this type of phase comparator is that it may lock to input frequencies close to the harmonics of the VCO centre frequency.



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PHASE COMPARATOR 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG\_IN and COMP\_IN are not important. PC2 comprises two D-type flip-flops, control gating and a 3-state output stage with sink and source transistors acting as current sources, henceforth called charge pump output of PC2. The circuit functions as an up-down counter (see Fig.5) where SIG\_IN causes an up-count and COMP\_IN a down count. The current switch charge pump output allows a virtually ideal performance of PC2, due to appliance of some pulse overlap of the up and down signals. See Fig.8a.

The pump current  $I_p$  is independent from the supply voltage and is set by the internal band gap reference of 2.5 V.

$$I_p = 17 \times \frac{2.5}{R_b} (A)$$

Where  $R_b$  is the external bias resistor between pin RB and ground.

The current and voltage transfer function of PC2 are shown in Fig.9.

The phase comparator gain is:

$$K_p = \frac{|I_p|}{2\pi} (A/r)$$

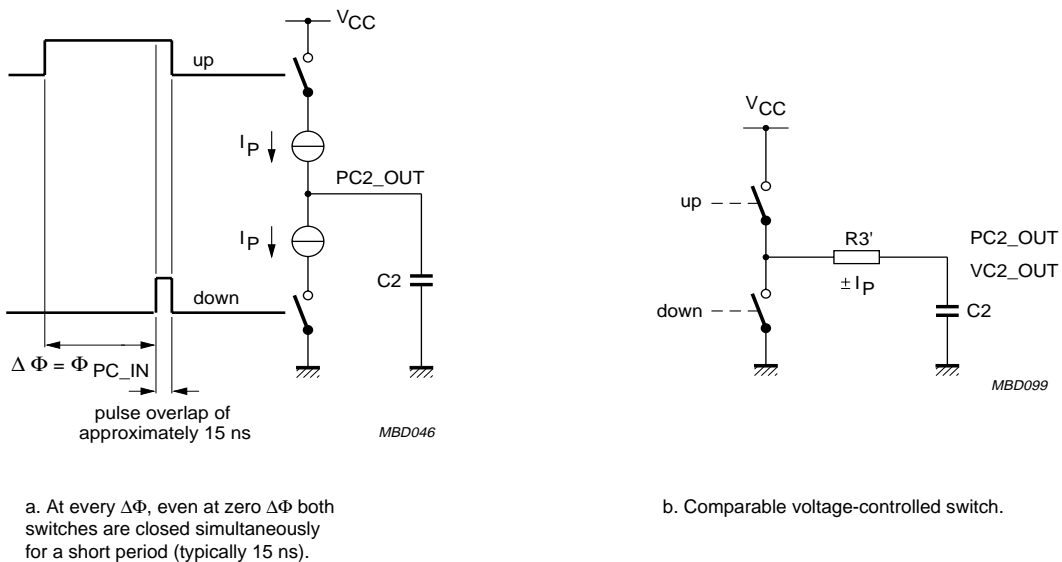
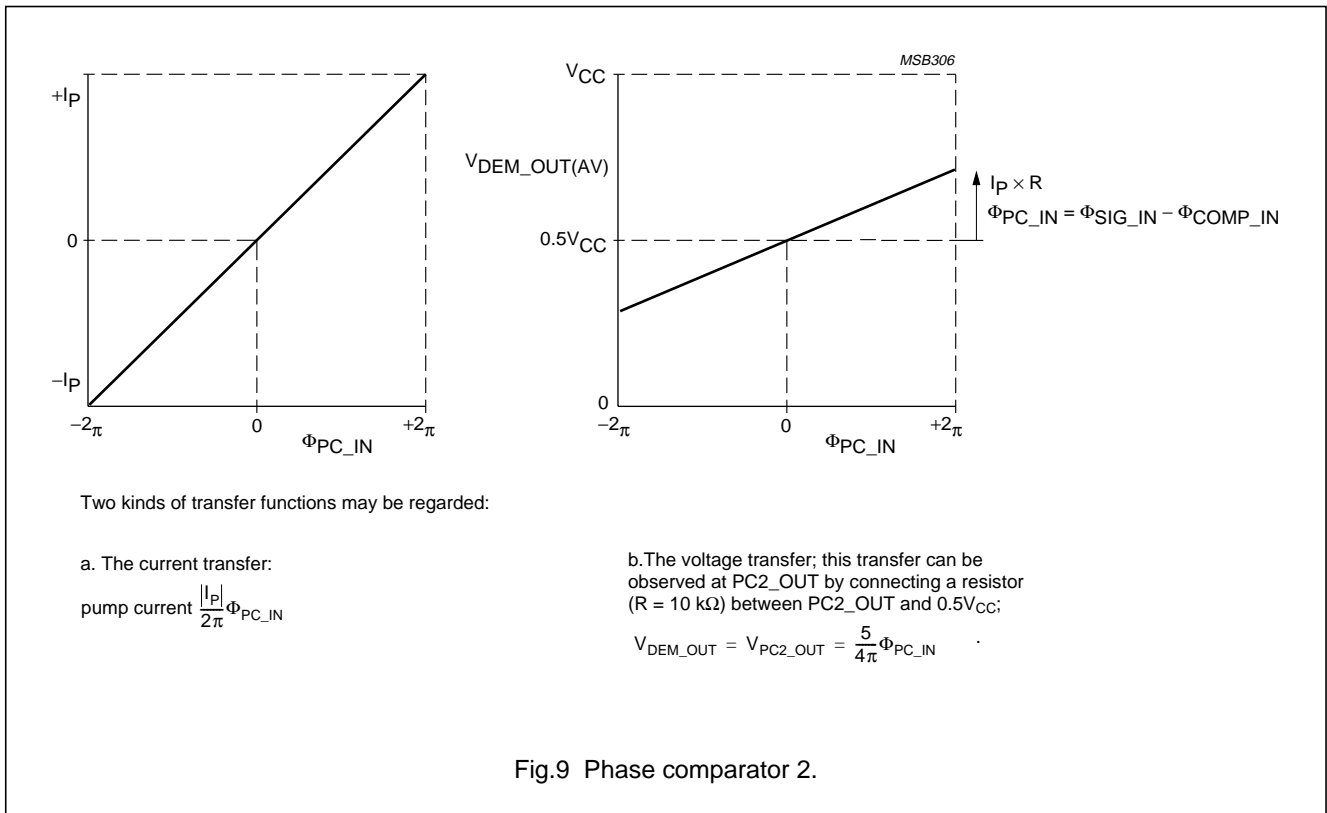


Fig.8 The current switch charge pump output of PC2.

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When the frequencies of SIG\_IN and COMP\_IN are equal but the phase of SIG\_IN leads that of COMP\_IN, the up output driver at PC2\_OUT is held 'ON' for a time corresponding to the phase difference ( $\Phi_{PC\_IN}$ ). When the phase of SIG\_IN lags that of COMP\_IN, the down or sink driver is held 'ON'.

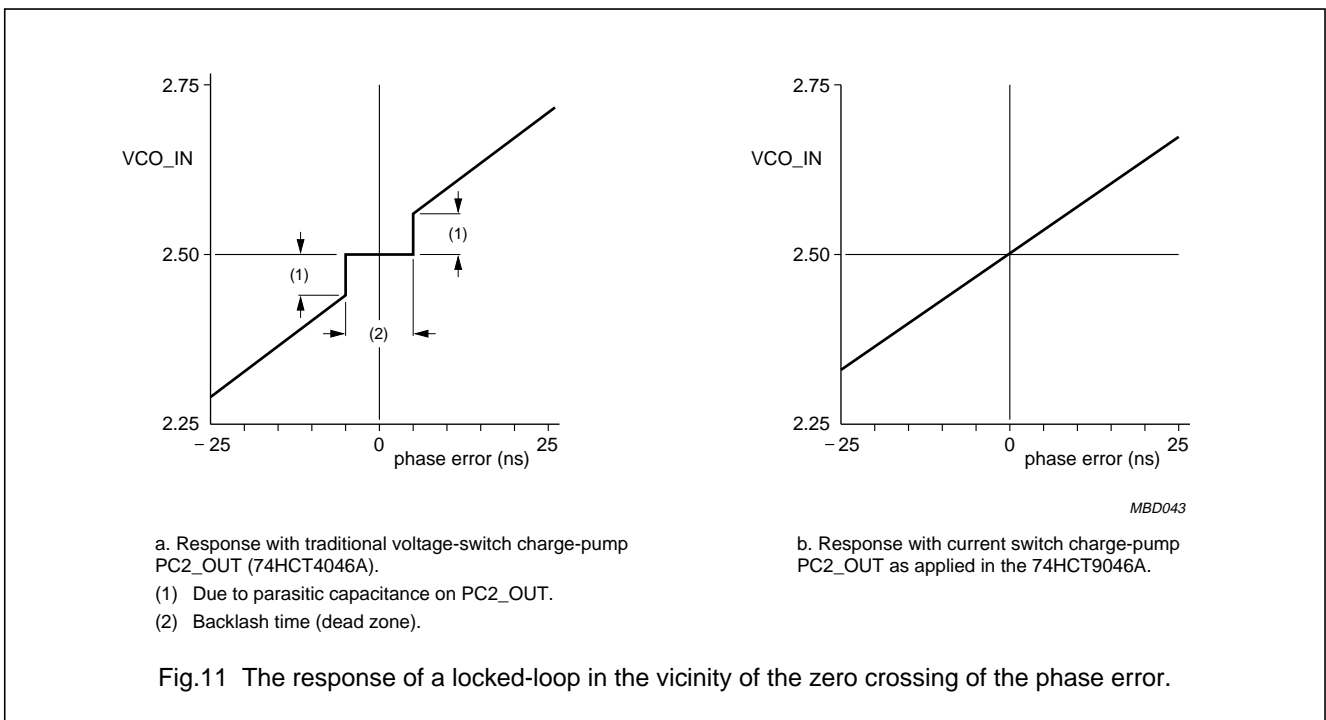
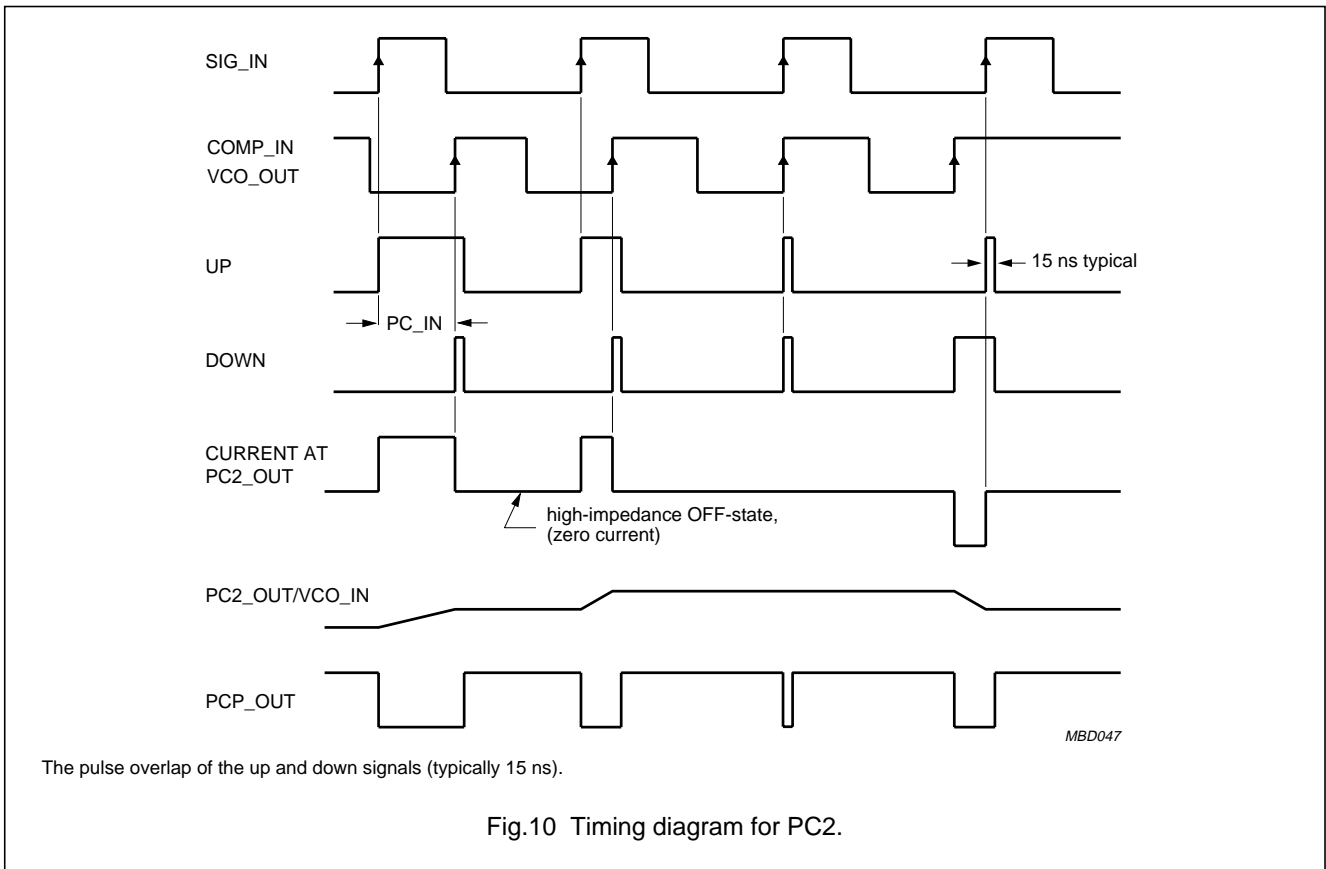
When the frequency of SIG\_IN is higher than that of COMP\_IN, the source output driver is held 'ON' for most of the input signal cycle time and for the remainder of the cycle time both drivers are 'OFF' (3-state). If the SIG\_IN frequency is lower than the COMP\_IN frequency, then it is the sink driver that is held 'ON' for most of the cycle. Subsequently the voltage at the capacitor (C2) of the low-pass filter connected to PC2\_OUT varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition the signal at the phase comparator pulse output (PCP\_OUT) has a minimum output pulse width equal to the overlap time, so can be used for indicating a locked condition.

Thus for PC2 no phase difference exists between SIG\_IN and COMP\_IN over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG\_IN the VCO adjust, via PC2, to its lowest frequency.

By using current sources as charge pump output on PC2, the dead zone or backlash time could be reduced to zero. Also, the pulse widening due to the parasitic output capacitance plays no role here. This enables a linear transfer function, even in the vicinity of the zero crossing. The differences between a voltage switch charge pump and a current switch charge pump are shown in Fig.11.

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The design of the low-pass filter is somewhat different when using current sources. The external resistor R3 is no longer present when using PC2 as phase comparator. The current source is set by  $R_b$ . A simple capacitor behaves as an ideal integrator now, because the capacitor is charged by a constant current. The transfer function of the voltage switch charge pump may be used. In fact it is even more valid, because the transfer function is no longer restricted for small changes only. Further the current is independent from both the supply voltage and the voltage across the filter. For one that is familiar with the low-pass filter design of the 74HCT4046A a relation may show how  $R_b$  relates with a fictive series resistance, called R3'.

This relation can be derived by assuming first that a voltage controlled switch PC2 of the 74HCT4046A is connected to the filter capacitance C2 via this fictive R3' (see Fig.8b). Then during the PC2 output pulse the charge current equals:

$$|I_p| = \frac{V_{CC} - V_{C2(0)}}{R3'}$$

With the initial voltage  $V_{C2(0)}$  at:

$$0.5V_{CC} = 2.5 \text{ V}, |I_p| = \frac{2.5}{R3'}$$

As shown before the charge current of the current switch of the 74HCT9046A is:

$$|I_p| = 17 \times \frac{2.5}{R_b}$$

Hence:

$$R3' = \frac{R_b}{17} (\Omega)$$

Using this equivalent resistance R3' for the filter design the voltage can now be expressed as a transfer function of PC2; assuming ripple ( $f_r = f_i$ ) is suppressed, as:

$$K_{PC2} = \frac{5}{4\pi} (V/r)$$

Again this illustrates the supply voltage independent behaviour of PC2.

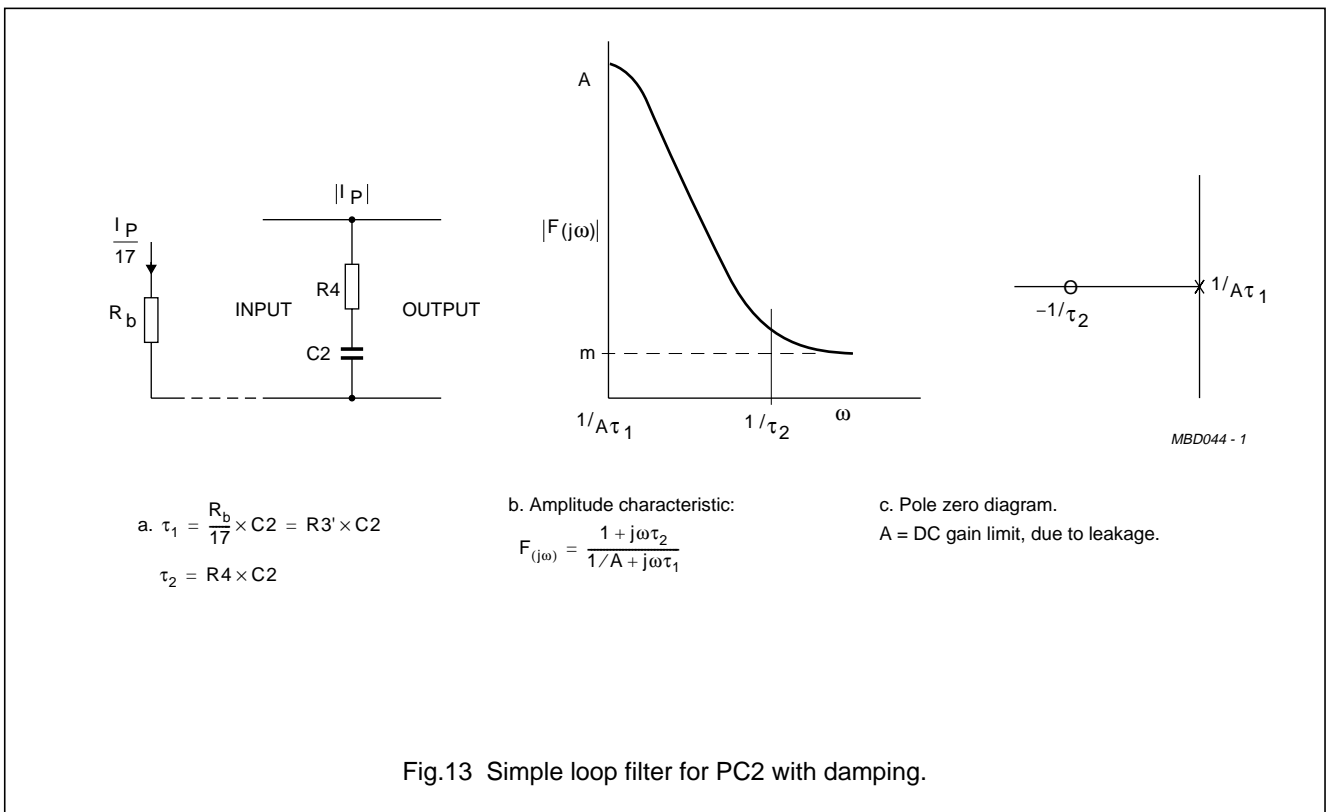
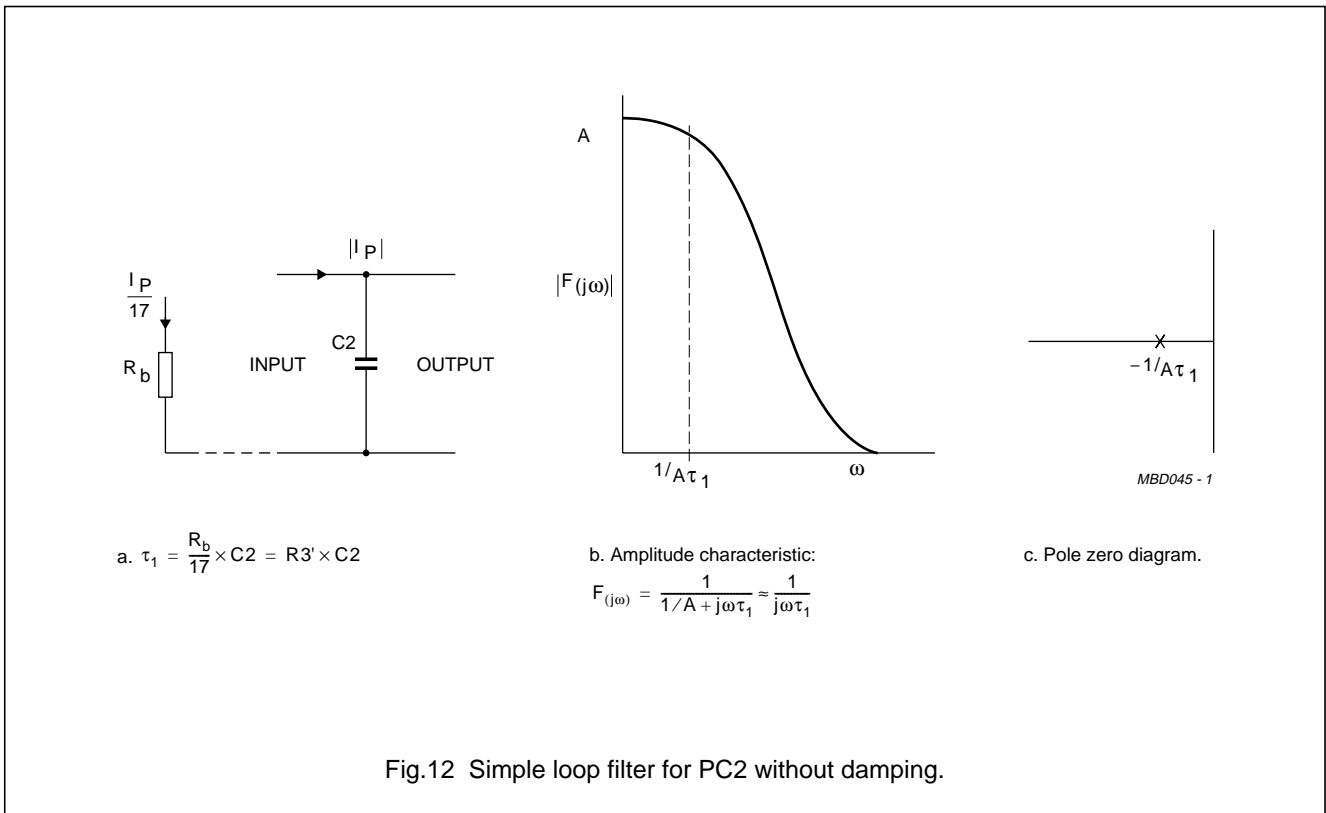
### LOOP FILTER COMPONENT SELECTION

Examples of PC2 combined with a passive filter are shown in Figs 12 and 13. Figure 12 shows that PC2 with only a C2 filter behaves as a high-gain filter. For stability the damped version of Fig.13 with series resistance R4 is preferred.

Practical design values for  $R_b$  are between 25 and 250 k $\Omega$  with  $R3' = 1.5$  to 15 k $\Omega$  for the filter design. Higher values for R3' require lower values for the filter capacitance which is very advantageous at low values the loop natural frequency  $\omega_n$ .

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC Characteristics	–40	–	+85	°C
			–40	–	+125	°C
$t_r, t_f$	input rise and fall times on pin INH	$V_{CC} = 4.5\text{ V}$	–	6	500	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7	V
$I_{IK}$	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
$I_O$	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	–	±25	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		–	±50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$			
	DIP16	note 1	–	750	mW
	SO16 and TSSOP16	note 2	–	500	mW

## Notes

- For DIP16 packages: above 70 °C derate linearly with 12 mW/K.
- For SO16 and TSSOP16 packages: above 70 °C derate linearly with 8 mW/K.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
PHASE COMPARATOR SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	2.4	–	V
V <sub>IL</sub>	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	2.1	1.35	V
V <sub>OH</sub>	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.98	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.26	V
I <sub>LI</sub>	input leakage current in pins SIG_IN and COMP_IN	V <sub>CC</sub> or GND	5.5	–	–	±30	µA
I <sub>OZ</sub>	3-state OFF-state current in pin PC2_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.5	µA
R <sub>I</sub>	input resistance SIG_IN, COMP_IN	V <sub>I</sub> at self-bias operating point; ΔV <sub>I</sub> = 0.5 V; see Figs 14 to 16	4.5	–	250	–	kΩ
R <sub>b</sub>	bias resistance		4.5	25	–	250	kΩ
I <sub>P</sub>	charge pump current	R <sub>b</sub> = 40 kΩ	4.5	±0.53	±1.06	±2.12	mA
VCO SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.98	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.26	V
V <sub>OL</sub>	LOW-level output voltage on pins C1A and C1B	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	4.5	–	–	0.40	V
I <sub>LI</sub>	input leakage current in pins INH and VCO_IN	V <sub>CC</sub> or GND	5.5	–	–	±0.1	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
R1	resistor value		4.5	3	–	300	kΩ
R2	resistor value		4.5	3	–	300	kΩ
C1	capacitance		4.5	40	–	no limit	pF
V <sub>VCO_IN</sub>	operating voltage on pin VCO_IN	over the range specified for R1	4.5	1.1	–	3.4	V
			5.0	1.1	–	3.9	V
			5.5	1.1	–	4.4	V
DEMODULATOR SECTION							
R <sub>s</sub>	resistor value	at R <sub>s</sub> > 300 kΩ the leakage current can influence V <sub>DEM_OUT</sub>	4.5	50	–	300	kΩ
V <sub>OFF</sub>	offset voltage VCO_IN to V <sub>DEM_OUT</sub>	V <sub>I</sub> = V <sub>VCO_IN</sub> = 0.5V <sub>CC</sub> ; values taken over R <sub>s</sub> range, see Fig.17	4.5	–	±20	–	mV
R <sub>dyn</sub>	dynamic output resistance at DEM_OUT	V <sub>DEM_OUT</sub> = 0.5V <sub>CC</sub>	4.5	–	25	–	Ω
GENERAL							
I <sub>CC</sub>	quiescent supply current (disabled)	pin INH at V <sub>CC</sub>	5.5	–	–	8.0	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	other inputs at V <sub>CC</sub> or GND; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V	4.5	–	100	360	μA
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
PHASE COMPARATOR SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	–	–	V
V <sub>IL</sub>	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	–	1.35	V
V <sub>OH</sub>	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.84	–	–	V
V <sub>OL</sub>	LOW-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.33	V
I <sub>LI</sub>	input leakage current in pins SIG_IN and COMP_IN	V <sub>CC</sub> or GND	5.5	–	–	±38	μA
I <sub>oz</sub>	3-state OFF-state current PC2_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±5.0	μA

## PLL with band gap controlled VCO

## 74HCT9046A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
VCO SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.84	–	–	V
V <sub>OL</sub>	LOW-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.33	V
V <sub>OL</sub>	LOW-level output voltage on pins C1A and C1B	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	4.5	–	–	0.47	V
I <sub>LI</sub>	input leakage current in pins INH and VCO_IN	V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
QUIESCENT SUPPLY CURRENT							
I <sub>CC</sub>	quiescent supply current (disabled)	pin INH at V <sub>CC</sub>	5.5	–	–	80.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	other inputs at V <sub>CC</sub> or GND; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V	4.5	–	–	450	µA
<b>T<sub>amb</sub> = –40 to +125 °C</b>							
PHASE COMPARATOR SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	3.15	–	–	V
V <sub>IL</sub>	LOW-level input voltage on pins SIG_IN and COMP_IN	DC coupled	4.5	–	–	1.35	V
V <sub>OH</sub>	HIGH-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage on pins PCP_OUT and PCn_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current in pins SIG_IN and COMP_IN	V <sub>CC</sub> or GND	5.5	–	–	±45	µA
I <sub>oz</sub>	3-state OFF-state current in pin PC2_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±10.0	µA

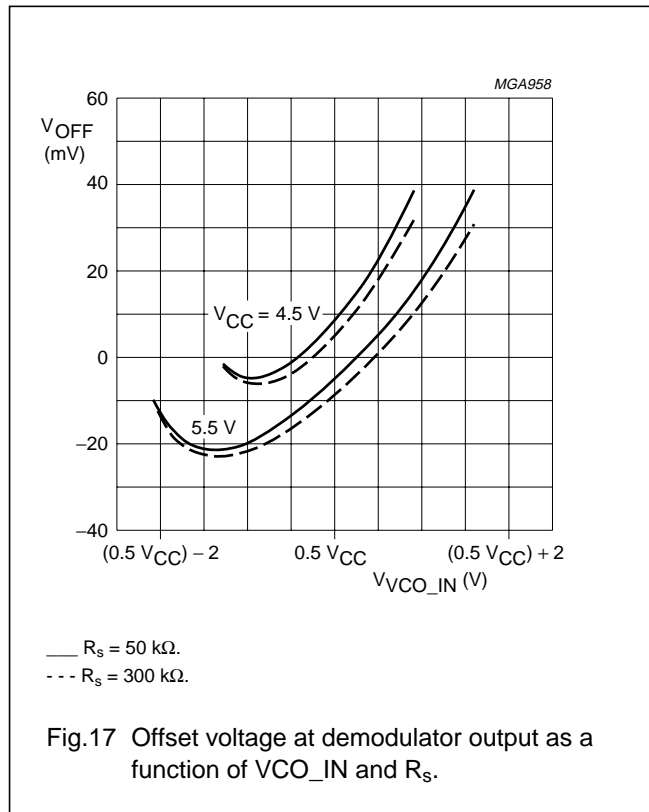
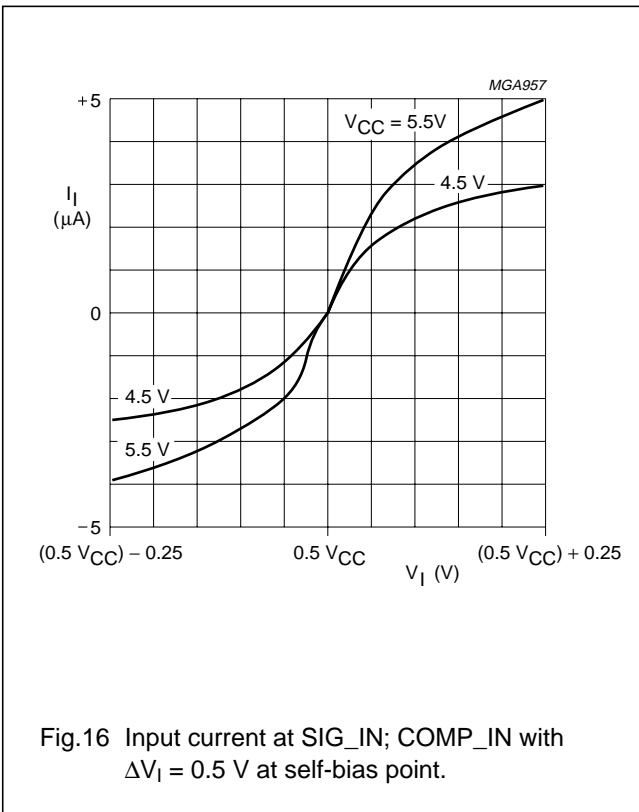
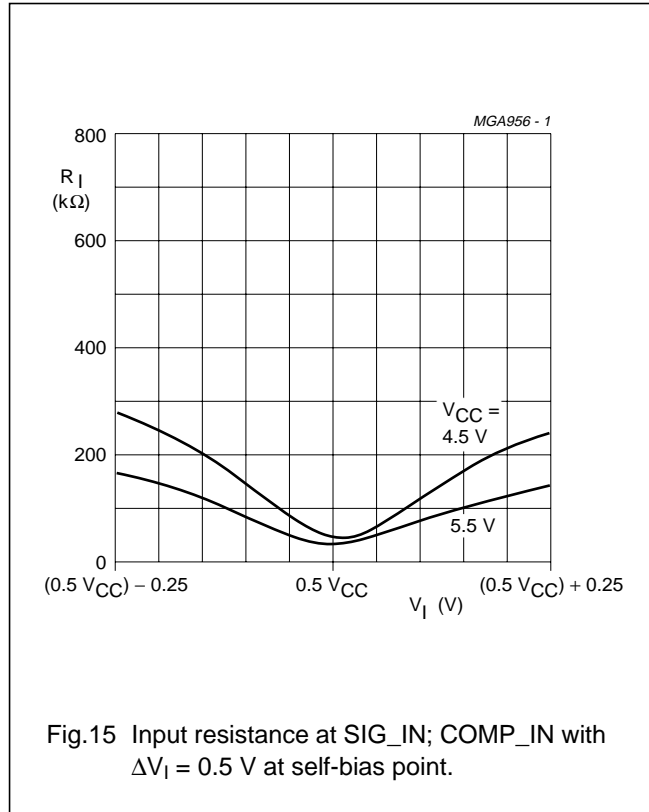
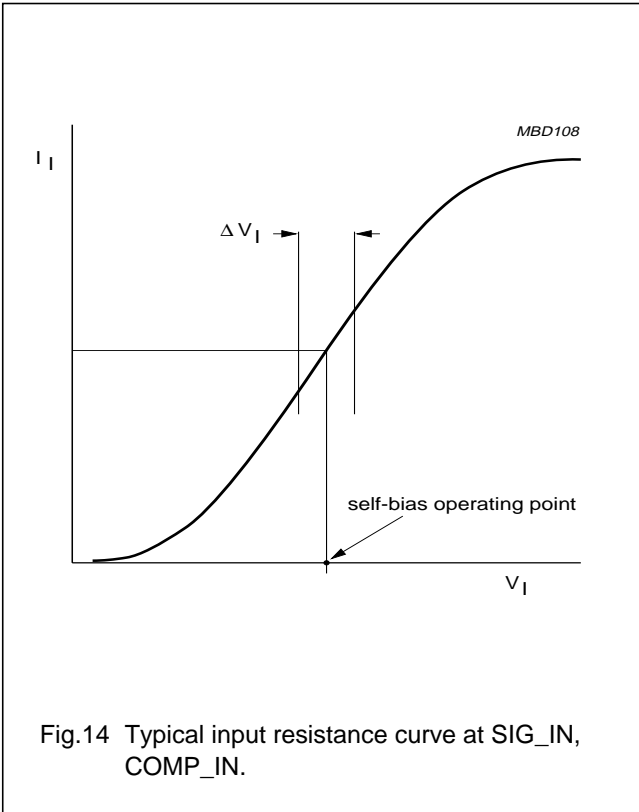
## PLL with band gap controlled VCO

## 74HCT9046A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
VCO SECTION							
V <sub>IH</sub>	HIGH-level input voltage on pin INH	DC coupled	4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage on pin INH	DC coupled	4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage on pin VCO_OUT	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
V <sub>OL</sub>	LOW-level output voltage on pins C1A and C1B	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 4.0 mA	4.5	–	–	0.54	V
I <sub>LI</sub>	input leakage current in pins INH and VCO_IN	V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
GENERAL							
I <sub>CC</sub>	quiescent supply current (disabled)	pin INH at V <sub>CC</sub>	5.5	–	–	160.0	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	other inputs at V <sub>CC</sub> or GND; V <sub>I</sub> = V <sub>CC</sub> – 2.1 V	4.5	–	–	490	µA

PLL with band gap controlled VCO

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## PLL with band gap controlled VCO

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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
PHASE COMPARATOR SECTION							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	23	40	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	35	68	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	30	56	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3–state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	36	65	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	Fig.18	4.5	–	7	15	ns
V <sub>i(p-p)</sub>	input sensitivity at pin SIGN_IN or COMP_IN (peak-to-peak value)	AC coupled; f <sub>i</sub> = 1 MHz	4.5	–	15	–	mV
VCO SECTION							
Δf <sub>c</sub>	centre frequency tolerance	V <sub>VCO_IN</sub> = 3.9 V; R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF	5.0	–10	–	+10	%
f <sub>c</sub>	VCO centre frequency	duty factor = 50%; V <sub>VCO_IN</sub> = 0.5V <sub>CC</sub> ; R1 = 4.3 kΩ; R2 = ∞; C1 = 40 pF; Figs 23 and 31	4.5	11.0	15.0	–	MHz
Δf <sub>VCO</sub>	VCO frequency linearity	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; Figs 24 and 25	4.5	–	0.4	–	%
δ <sub>VCO</sub>	duty factor at VCO_OUT		4.5	–	50	–	%

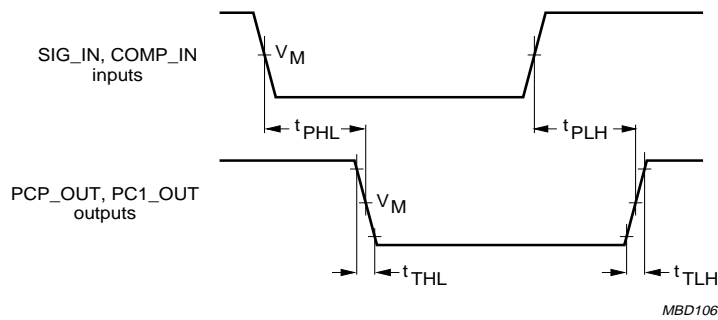
## PLL with band gap controlled VCO

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SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
PHASE COMPARATOR SECTION							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	–	50	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	–	85	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	70	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	81	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	Fig.18	4.5	–	–	19	ns
VCO SECTION							
Δf/T	frequency stability with temperature change	V <sub>VCO_IN</sub> = 0.5V <sub>CC</sub> ; recommended range: R1 = 10 kΩ; R2 = 10 kΩ; C1 = 1 nF; see Figs 20 to 22	4.5	0.06	–	–	%/K
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
PHASE COMPARATOR SECTION							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay SIG_IN, COMP_IN to PC1_OUT	Fig.18	4.5	–	–	60	ns
	propagation delay SIG_IN, COMP_IN to PCP_OUT	Fig.18	4.5	–	–	102	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	84	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output enable time SIG_IN, COMP_IN to PC2_OUT	Fig.19	4.5	–	–	98	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	Fig.18	4.5	–	–	22	ns

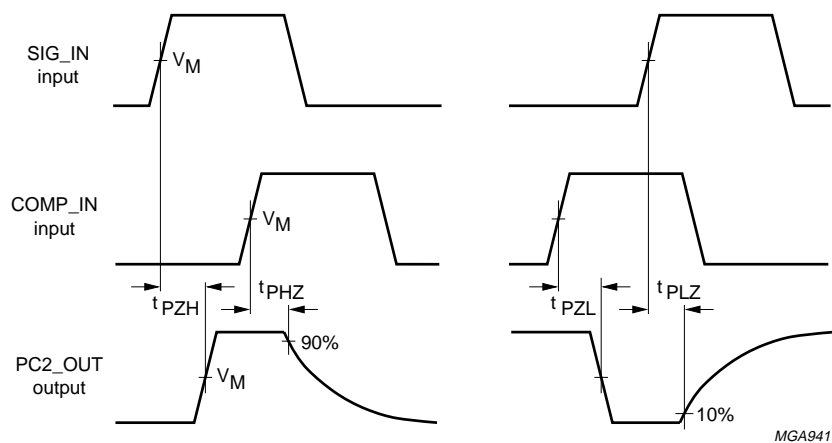
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$V_M = 0.5V_{CC}$ ;  $V_I = \text{GND to } V_{CC}$ .

Fig.18 Waveforms showing input (SIG\_IN and COMP\_IN) to output (PCP\_OUT and PC1\_OUT) propagation delays and the output transition times.

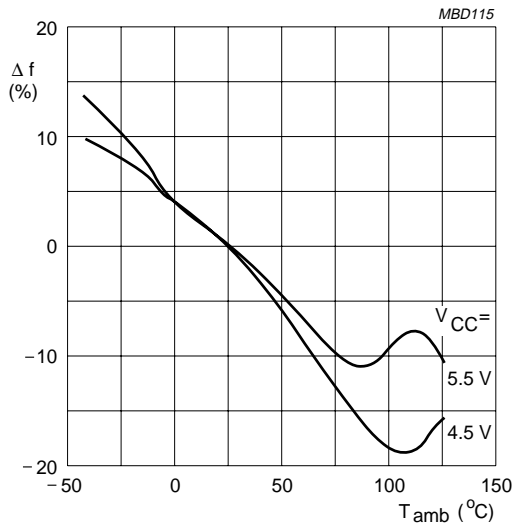


$V_M = 0.5V_{CC}$ ;  $V_I = \text{GND to } V_{CC}$ .

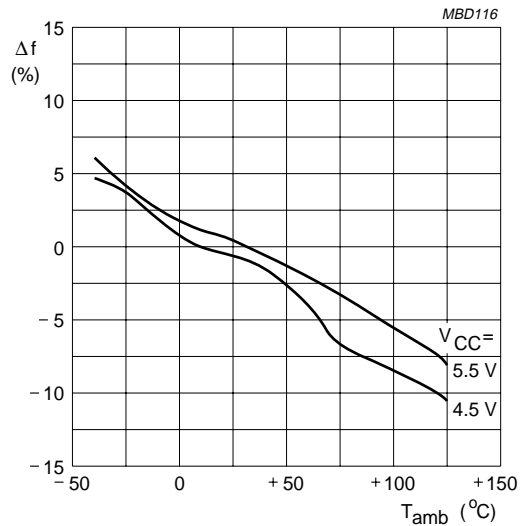
Fig.19 Waveforms showing the 3-state enable and disable times for PC2\_OUT.

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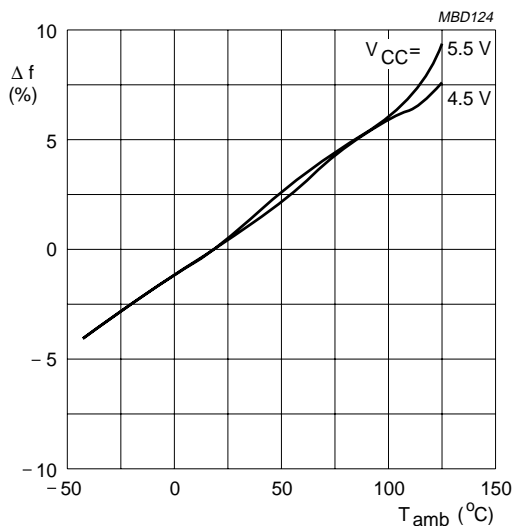


a.  $R1 = 3\text{ k}\Omega$ ;  $R2 = \infty$ ;  $C1 = 100\text{ pF}$ .

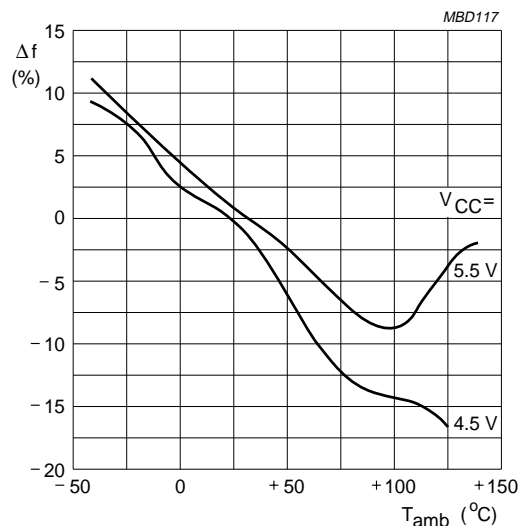


b.  $R1 = 10\text{ k}\Omega$ ;  $R2 = \infty$ ;  $C1 = 100\text{ pF}$ .

Fig.20 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.



a.  $R1 = 300\text{ k}\Omega$ ;  $R2 = \infty$ ;  $C1 = 100\text{ pF}$ .

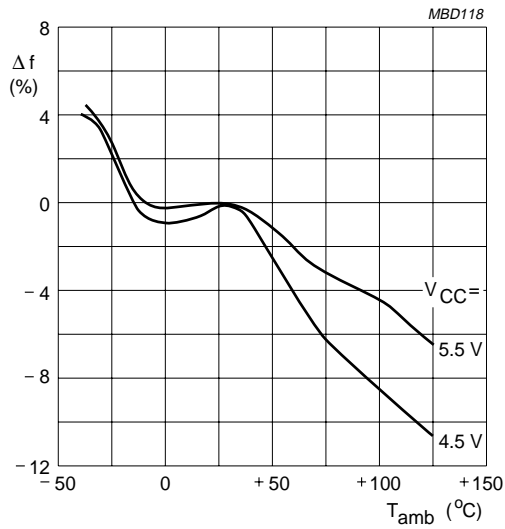


b.  $R1 = \infty$ ;  $R2 = 3\text{ k}\Omega$ ;  $C1 = 100\text{ pF}$ .

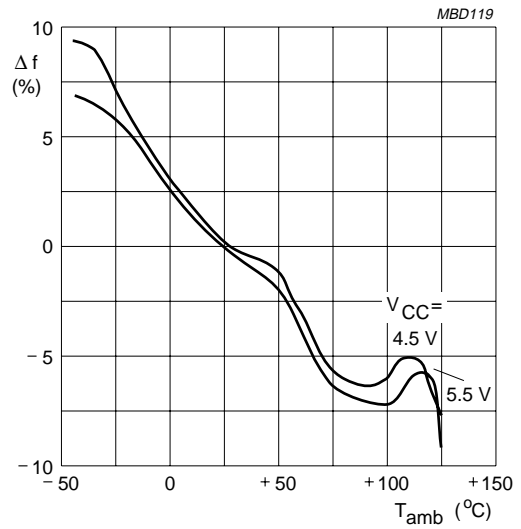
Fig.21 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

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a. R1 = ∞; R2 = 10 kΩ; C1 = 100 pF.

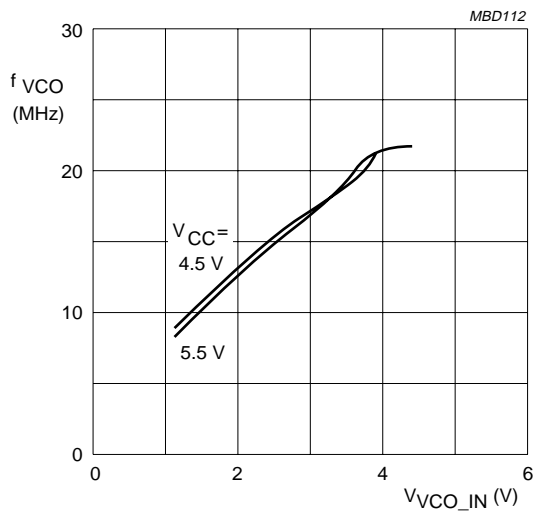


b. R1 = ∞; R2 = 300 kΩ; C1 = 100 pF.

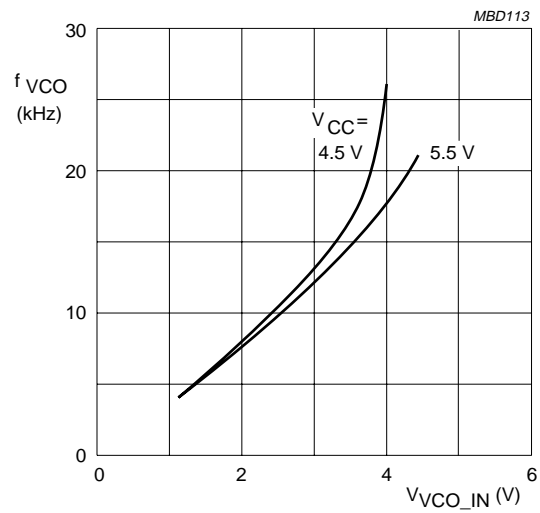
Fig.22 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

PLL with band gap controlled VCO

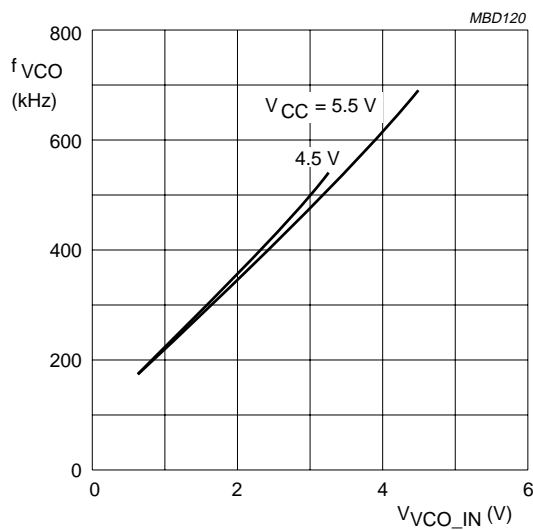
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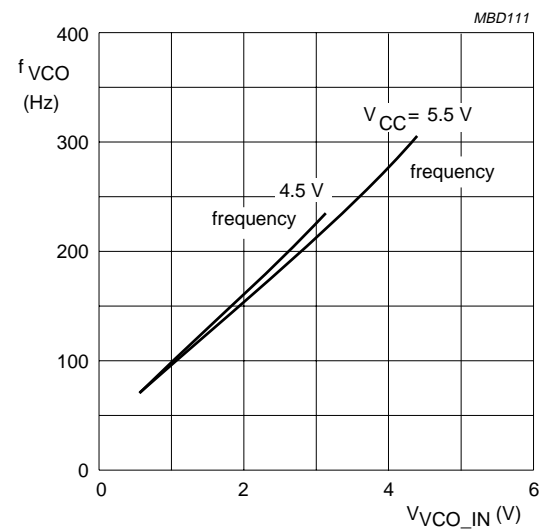
a.  $R1 = 4.3\text{ k}\Omega$ ;  $C1 = 39\text{ pF}$ .



b.  $R1 = 4.3\text{ k}\Omega$ ;  $C1 = 100\text{ nF}$ .



c.  $R1 = 300\text{ k}\Omega$ ;  $C1 = 39\text{ pF}$ .

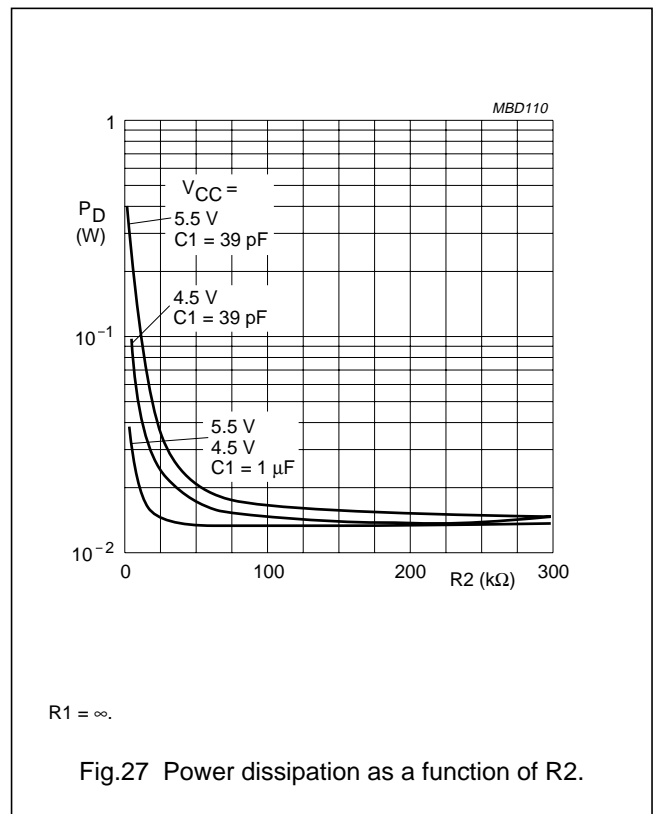
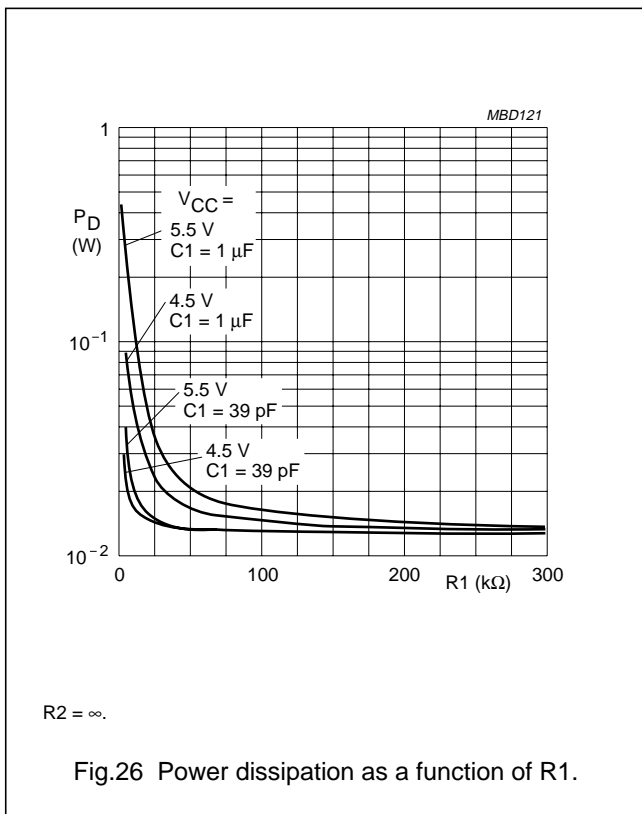
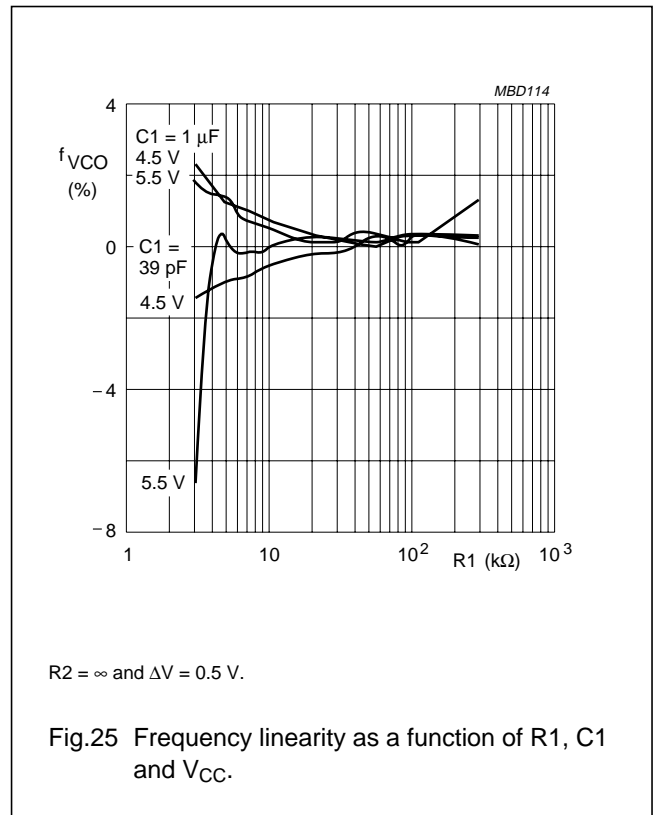
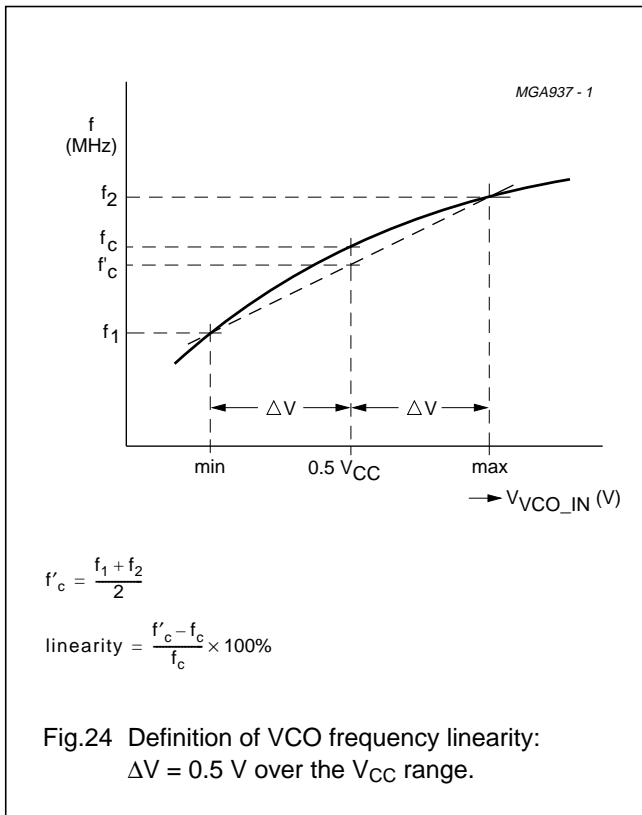


d.  $R1 = 300\text{ k}\Omega$ ;  $C1 = 100\text{ nF}$ .

Fig.23 Graphs showing VCO frequency as a function of the VCO input voltage ( $V_{VCO\_IN}$ ).

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PLL with band gap controlled VCO

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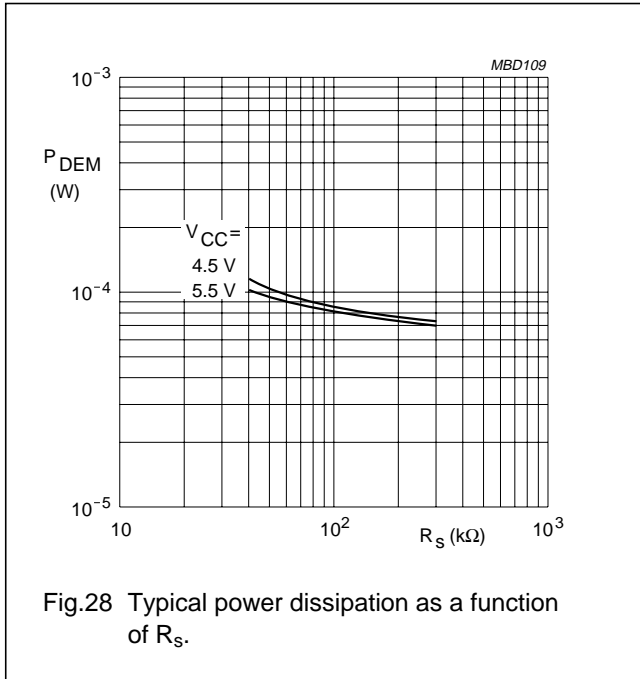


Fig.28 Typical power dissipation as a function of  $R_S$ .

**APPLICATION INFORMATION**

This information is a guide for the approximation of values of external components to be used with the 74HCT9046A in a phase-locked-loop system.

Values of the selected components should be within the ranges shown in Table 1.

**Table 1** Survey of components.

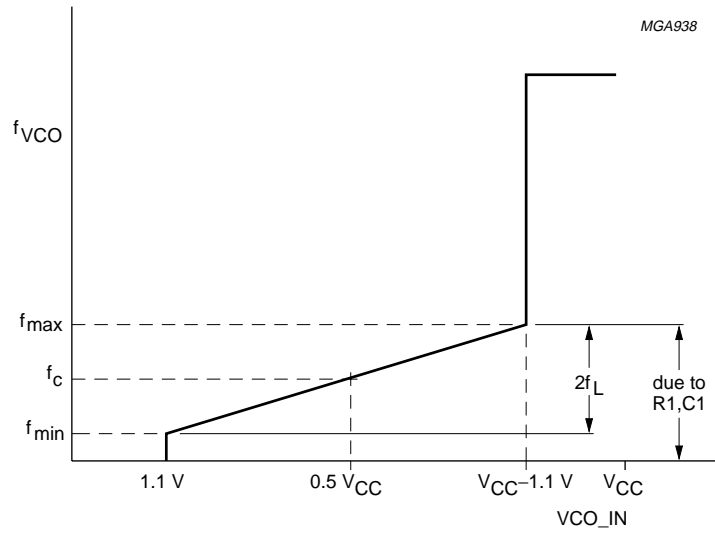
COMPONENT	VALUE
R1	between 3 kΩ and 300 kΩ
R2	between 3 kΩ and 300 kΩ
R1 + R2	parallel value >2.7 kΩ
C1	>40 pF

**Table 2** Design considerations for VCO section.

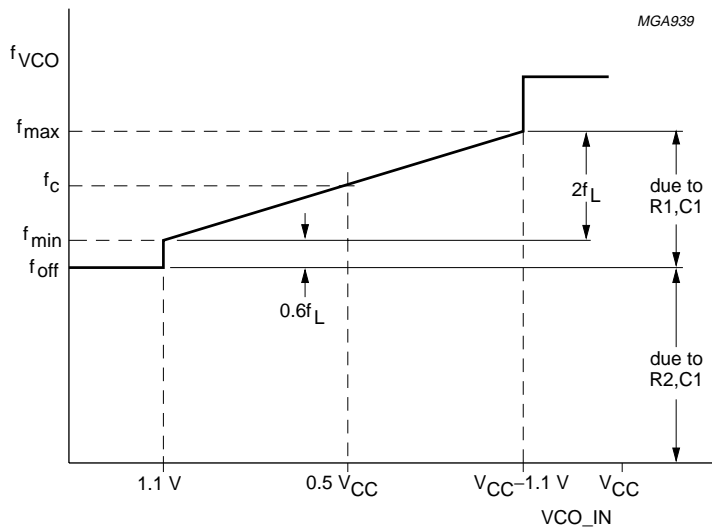
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
VCO frequency <b>without extra offset</b>	PC1, PC2	VCO frequency characteristic. With $R_2 = \infty$ and $R_1$ within the range $3\text{ k}\Omega < R_1 < 300\text{ k}\Omega$ , the characteristics of the VCO operation will be as shown in Fig.29a. (Due to $R_1$ , $C_1$ time constant a small offset remains when $R_2 = \infty$ ).
	PC1	Selection of $R_1$ and $C_1$ . Given $f_c$ , determine the values of $R_1$ and $C_1$ using Fig.31.
	PC2	Given $f_{max}$ and $f_c$ determine the values of $R_1$ and $C_1$ using Fig.31; use Fig.33 to obtain $2f_L$ and then use this to calculate $f_{min}$ .
VCO frequency <b>with extra offset</b>	PC1, PC2	VCO frequency characteristic. With $R_1$ and $R_2$ within the ranges $3\text{ k}\Omega < R_1 < 300\text{ k}\Omega < R_2 < 300\text{ k}\Omega$ , the characteristics of the VCO operation is as shown in Fig.29b.
	PC1, PC2	Selection of $R_1$ , $R_2$ and $C_1$ . Given $f_c$ and $f_L$ determine the value of product $R_1C_1$ by using Fig.33. Calculate $f_{off}$ from the equation $f_{off} = f_c - 1.6f_L$ . Obtain the values of $C_1$ and $R_2$ by using Fig.32. Calculate the value of $R_1$ from the value of $C_1$ and the product $R_1C_1$ .
PLL conditions with no signal at pin SIG_IN	PC1	VCO adjusts to $f_c$ with $\Phi_{PC\_IN} = 90^\circ$ and $V_{VCO\_IN} = 0.5V_{CC}$ .
	PC2	VCO adjusts to $f_{offset}$ with $\Phi_{PC\_IN} = -360^\circ$ and $V_{VCO\_IN} = \text{minimum}$ .

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a. Operating without offset;  
 $f_c$  = centre frequency;  
2 $f_L$  = frequency lock range.



b. Operating with offset;  
 $f_c$  = centre frequency;  
2 $f_L$  = frequency lock range.

Fig.29 Frequency characteristic of VCO.

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**Filter design considerations for PC1 and PC2 of the 74HCT9046A**

Figure 30 shows some examples of passive and active filters to be used with the phase comparators of the 74HCT9046A. Transfer functions of phase comparators and filters are given in Table 3.

**Table 3** Transfer functions of phase comparators and filters.

PHASE COMPARATOR	EXPLANATION	FIGURE	FILTER TYPE	TRANSFER FUNCTION
PC1	$K_{PC1} = \frac{V_{CC}}{\pi} V/r$	30a.	passive filter without damping	$F_{(j\omega)} = \frac{1}{1 + j\omega\tau_1}$
	$\tau_1 = R3 \times C2;$ $\tau_2 = R4 \times C2;$ $\tau_3 = R4 \times C3;$ $A = 10^5 = \text{DC gain amplitude}$	30b.	passive filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$
		30c.	active filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$
PC2	$K_{PC2} = \frac{5}{4\pi} V/r$  $\tau_1 = R3' \times C2;$ $\tau_2 = R4 \times C2;$ $\tau_3 = R4 \times C3;$ $R3' = R_b/17;$ $R_b = 25 \text{ to } 250 \text{ k}\Omega$	30d.	passive filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$  $A = 10^5 = \text{DC gain amplitude}$
		30e.	active filter with damping	$F_{(j\omega)} = \frac{1 + j\omega\tau_2}{1/A + j\omega\tau_1} \approx \frac{1 + j\omega\tau_2}{j\omega\tau_1}$  $A = 10^5 = \text{DC gain amplitude}$

**General design consideration.**

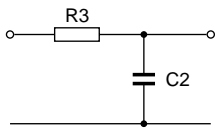
SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATION
PLL locks on harmonics at centre frequency	PC1	yes
	PC2	no
Noise rejection at signal input	PC1	high
	PC2	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$ ; large ripple content at $\Phi_{PC\_IN} = 90^\circ$
	PC2	$f_r = f_i$ ; small ripple content at $\Phi_{PC\_IN} = 0^\circ$

PLL with band gap controlled VCO

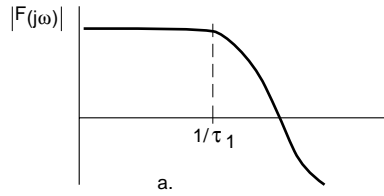
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PC1

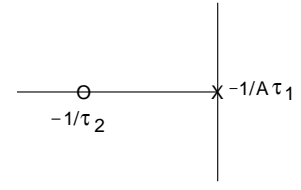
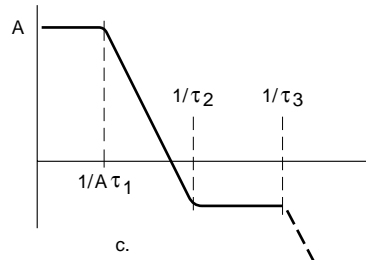
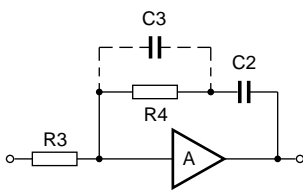
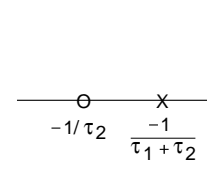
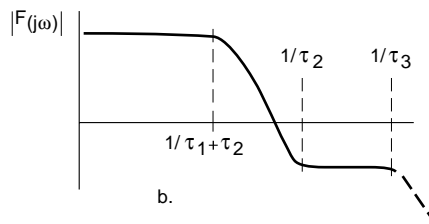
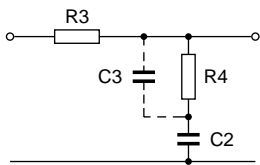
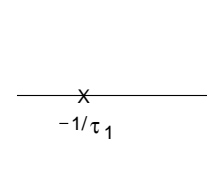
CIRCUIT



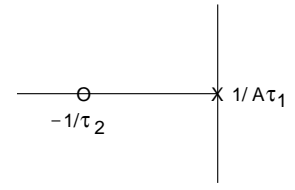
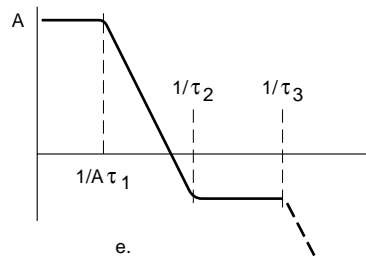
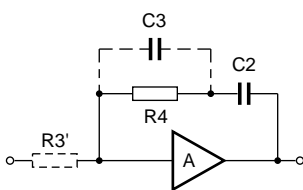
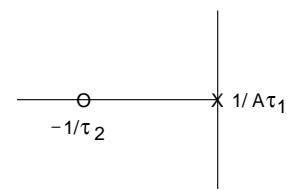
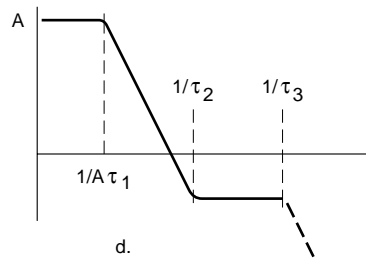
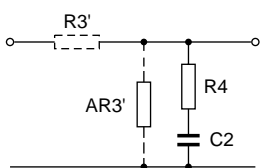
AMPLITUDE CHARACTERISTIC



POLE ZERO DIAGRAM



PC2

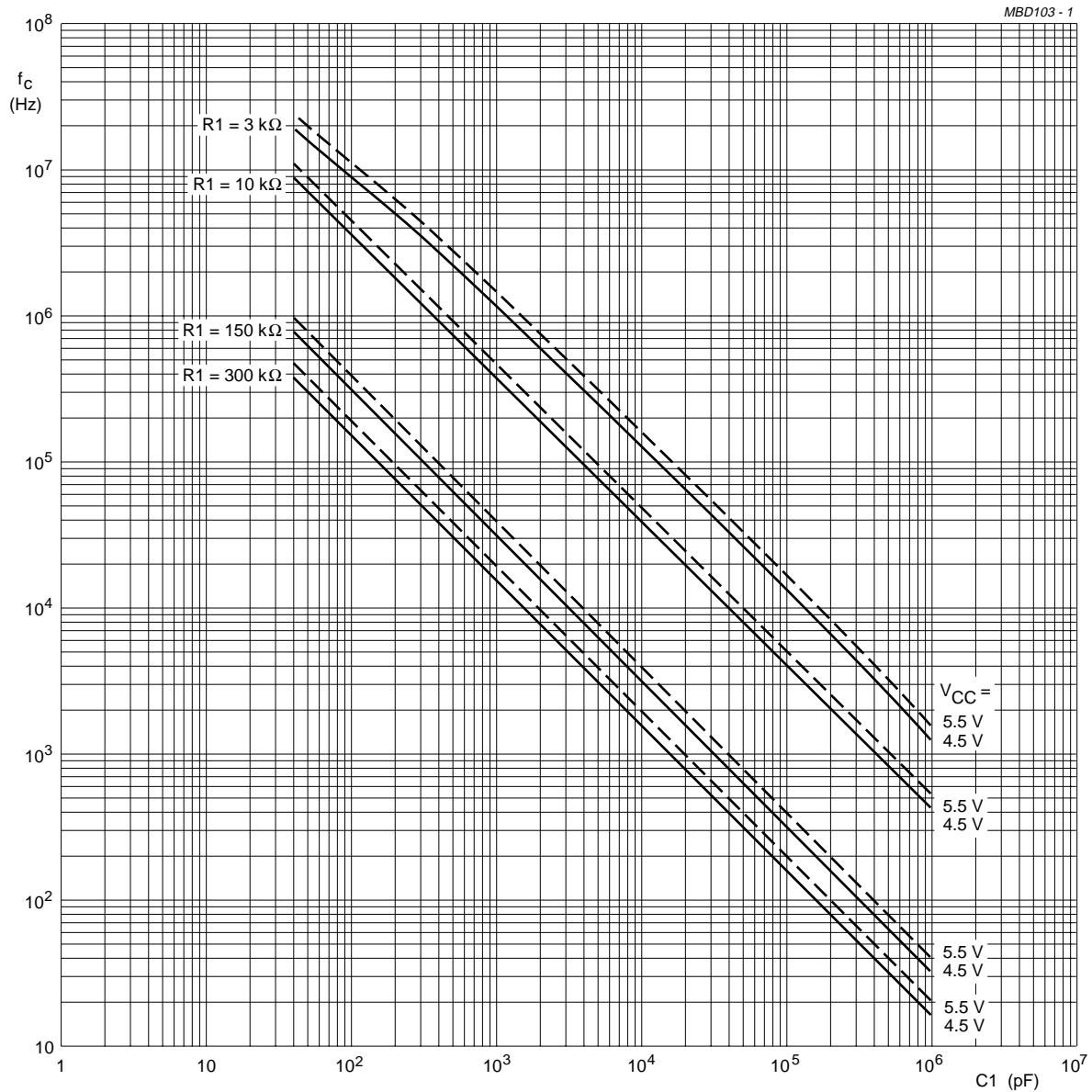


MBD107 - 1

Fig.30 Passive and active filters for 74HCT9046A.

PLL with band gap controlled VCO

74HCT9046A

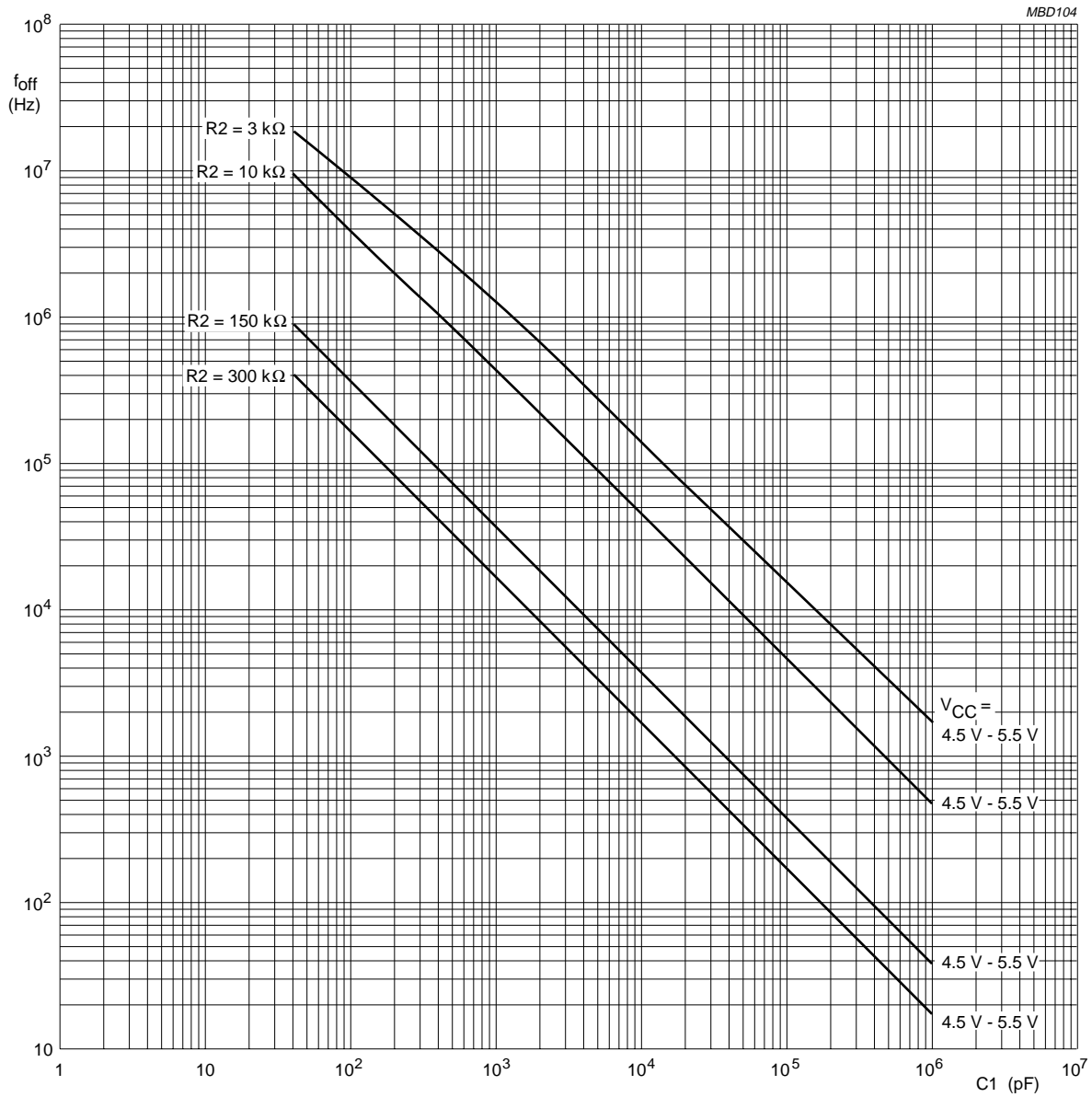


$R_2 = \infty$ ;  $V_{VCO\_IN} = 0.5V_{CC}$ ;  $INH = GND$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

Fig.31 Typical value of VCO centre frequency ( $f_c$ ) as a function of  $C_1$ .

PLL with band gap controlled VCO

74HCT9046A

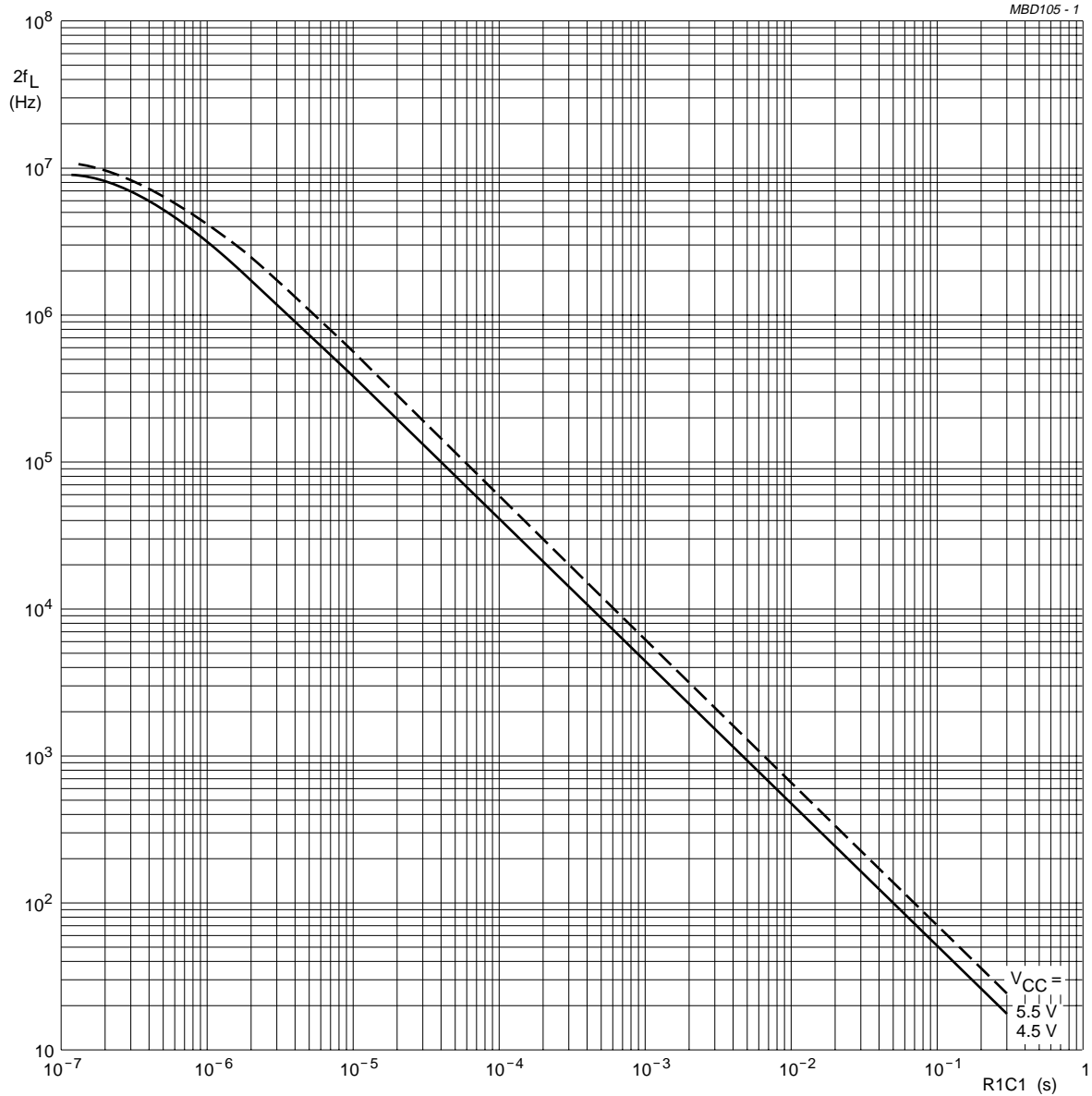


R1 = ∞; V<sub>VCO\_IN</sub> = 0.5V<sub>CC</sub>; INH = GND; T<sub>amb</sub> = 25 °C.

Fig.32 Typical value of frequency offset as a function of C1.

PLL with band gap controlled VCO

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$$K_v = \frac{2f_L}{V_{VCO\_IN\ range}} 2\pi(r/s/V)$$

$V_{VCO\_IN} = 1.1 \text{ to } (V_{CC} - 1.1) \text{ V}$

Fig.33 Typical frequency lock range  $2f_L$  as a function of the product R1 and C1.

PLL with band gap controlled VCO

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**PLL design example**

The frequency synthesizer used in the design example shown in Fig.34 has the following parameters:

- Output frequency: 2 MHz to 3 MHz.
- Frequency steps: 100 kHz.
- Settling time: 1 ms.
- Overshoot: <20%.

The open loop gain is:

$$H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$$

and the closed loop:

$$\frac{\Phi_u}{\Phi_i} = \frac{K_p \times K_f \times K_o \times K_n}{1 + K_p \times K_f \times K_o \times K_n}$$

where:

- $K_p$  = phase comparator gain
- $K_f$  = low-pass filter transfer gain
- $K_o$  =  $K_v/s$  VCO gain
- $K_n$  =  $1/n$  divider ratio.

The programmable counter ratio  $K_n$  can be found as follows:

$$N_{min} = \frac{f_{OUT}}{f_{step}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{max} = \frac{f_{OUT}}{f_{step}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1; R2 = 10 kΩ (adjustable).

The values can be determined using the information in Table 2.

With  $f_c = 2.5 \text{ MHz}$  and  $f_L = 500 \text{ kHz}$  this gives the following values

( $V_{CC} = 5.0 \text{ V}$ ):

- R1 = 30 kΩ.
- R2 = 30 kΩ.
- C1 = 100 pF.

The VCO gain is:

$$K_v = \frac{2f_L \times 2\pi}{(V_{CC} - 1.1) - 1.1} = \frac{1 \text{ MHz}}{2.8} \times 2\pi \approx 2.24 \times 10^6 \text{ r/s/V}$$

The gain of the phase comparator PC2 is:

$$K_p = \frac{5}{4 \times \pi} = 0.4 \text{ V/r}$$

Using PC2 with the passive filter as shown in Fig.34 results in a high gain loop with the same performance as a loop with an active filter. Hence loop filter equations as for a high gain loop should be used. The current source output of PC2 can be simulated then with a fictive filter resistance:

$$R3' = \frac{R_b}{17}$$

The transfer functions of the filter is given by:

$$K_f = \frac{1 + s\tau_2}{s\tau_2}$$

Where:

- $\tau_1 = R3' \times C2.$
- $\tau_2 = R4 \times C2.$

The characteristic equation is:  $1 + K_p \times K_f \times K_o \times K_n$

This results in:

$$1 + K_p \left( \frac{1 + s\tau_2}{s\tau_1} \right) \frac{K_v}{s} K_n = 0$$

or:

$$s^2 + sK_p K_v K_n \frac{\tau_2}{\tau_1} + K_p K_v K_n / \tau_1 = 0$$

This can be written as:

$$s^2 + 2\zeta\omega_n s + (\omega_n)^2 = 0$$

with the natural frequency  $\omega_n$  defined as:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{\tau_1}}$$

and the damping value given as:  $\zeta = 0.5 \times \tau_2 \times \omega_n$

In Fig.35 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine  $\omega_n$ . From Fig.35 it can be seen that the damping ratio  $\zeta = 0.707$  will produce an overshoot of less than 20% and settle to within 5% at  $\omega_n t = 5$ . The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \text{ r/s}.$$

PLL with band gap controlled VCO

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Rewriting the equation for natural frequency results in:

$$\tau_1 = \frac{K_p \times K_v \times K_n}{(\omega_n)^2}$$

The maximum overshoot occurs at  $N_{max} = 30$ ; hence  $K_n = 1/30$ :

$$\tau_1 = \frac{0.4 \times 2.24 \times 10^6}{5000^2 \times 30} = 0.0012$$

When  $C2 = 470$  nF, it follows:

$$R3' = \frac{\tau_1}{C2} = \frac{0.0012}{470 \times 10^{-9}} = 2550 \Omega$$

Hence the current source bias resistance

$$R_b = 17 \times 2550 = 43 \text{ k}\Omega.$$

With  $\zeta = 0.707$  ( $0.5 \times \tau_2 \times \omega_n$ ) it follows:

$$\tau_2 = \frac{0.707}{0.5 \times 5000} = 0.00028$$

$$R4 = \frac{\tau_2}{C2} = \frac{0.00028}{470 \times 10^{-9}} = 600 \Omega$$

For extra ripple suppression a capacitor  $C3$  can be connected in parallel with  $R4$ , with an extra  $\tau_3 = R4 \times C3$ .

For stability reasons  $\tau_3$  should be  $< 0.1\tau_2$ , hence  $C3 < 0.1C2$  or  $C3 = 39$  nF.

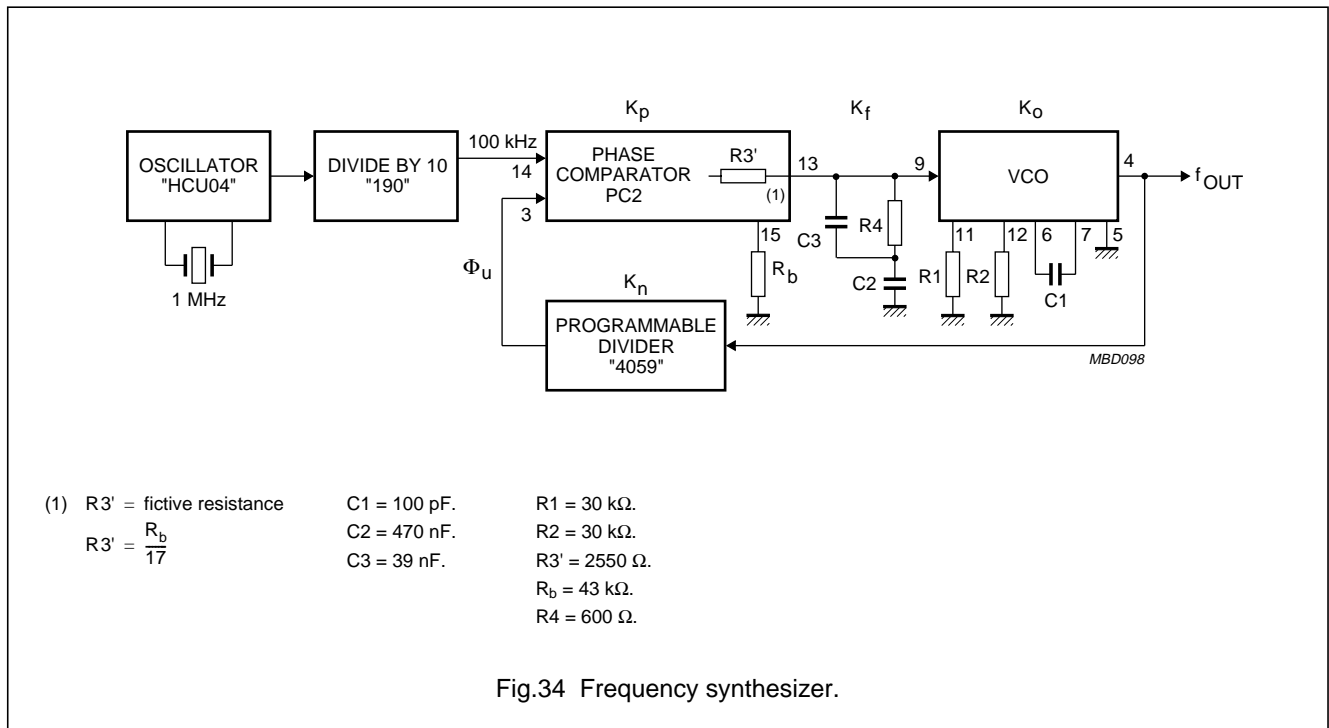


Fig.34 Frequency synthesizer.

PLL with band gap controlled VCO

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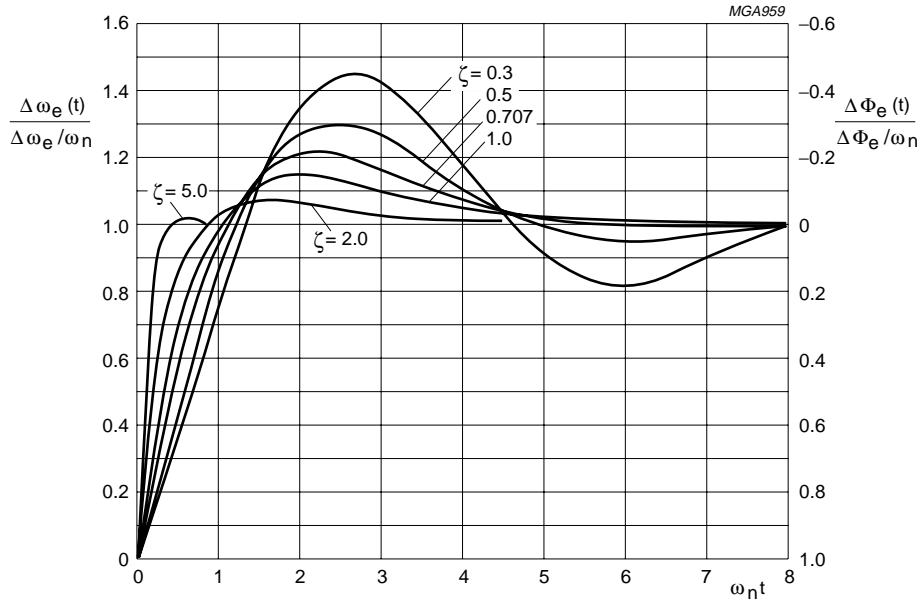


Fig.35 Type 2, second order frequency step response.

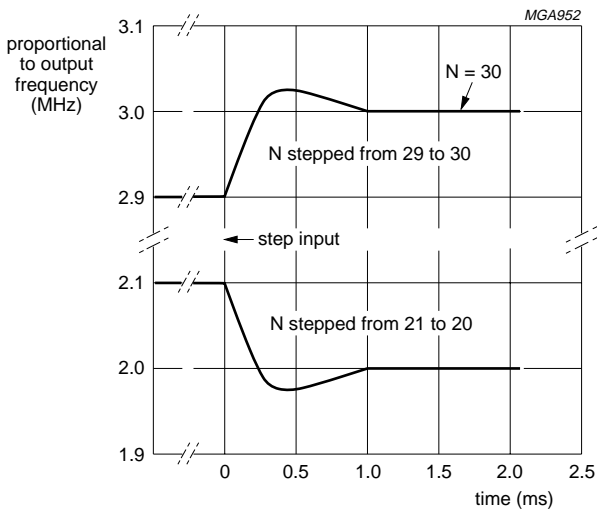


Fig.36 Frequency compared to the time response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin VCO\_IN of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin VCO\_IN with a simple RC filter, whose time constant is long compared with the phase detector sampling rate but short compared with the PLL response time.

**Further information**

For an extensive description and application example please refer to "Application note" ordering number 9397 750 00078.

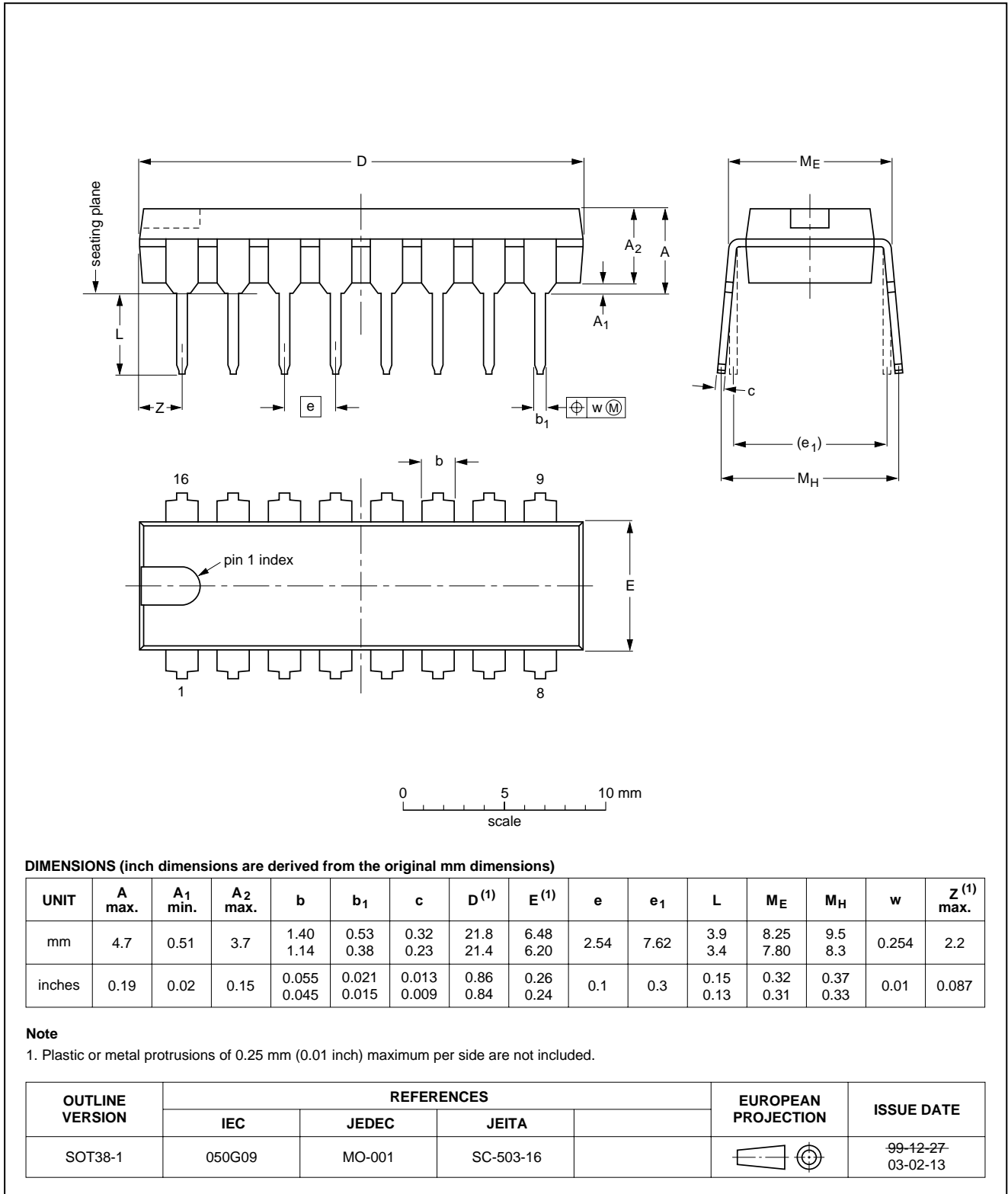
PLL with band gap controlled VCO

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PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

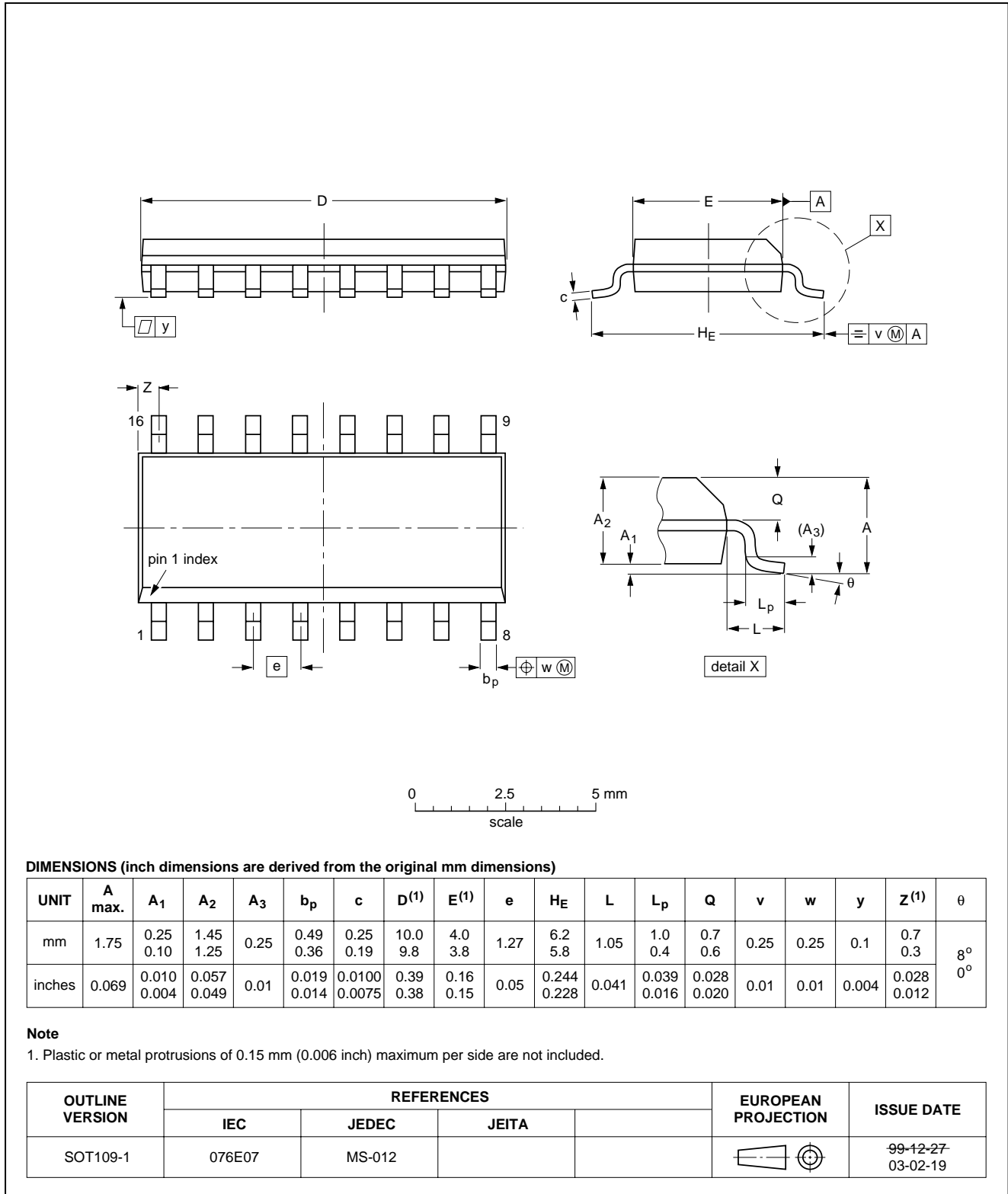


PLL with band gap controlled VCO

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

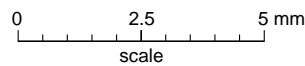
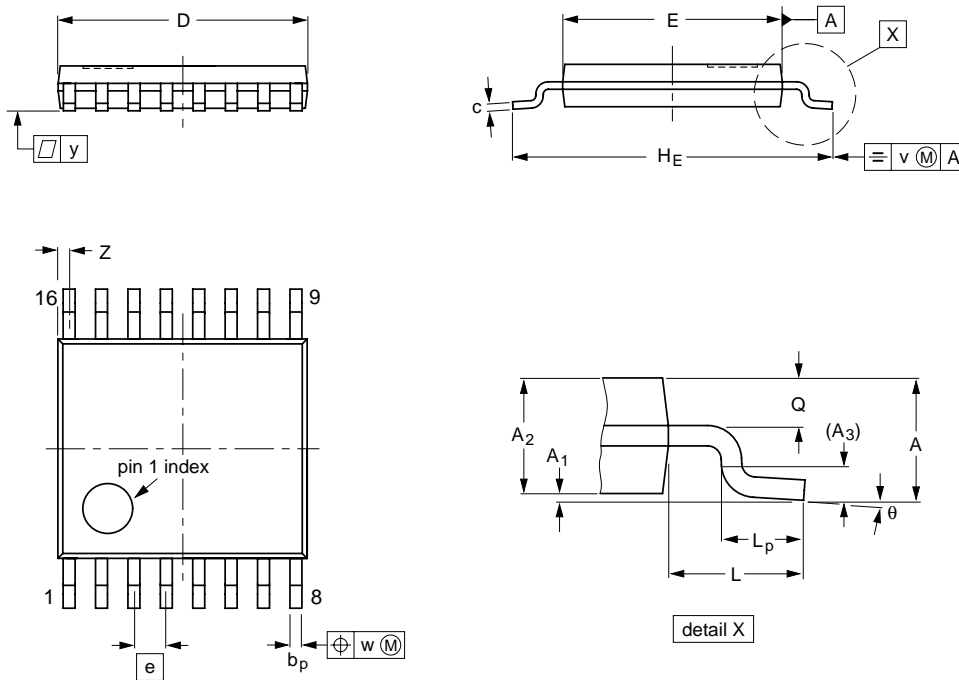


PLL with band gap controlled VCO

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

## PLL with band gap controlled VCO

74HCT9046A

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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