

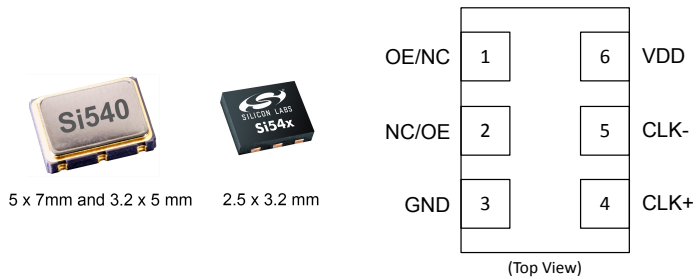
Ultra Series™ 晶体振荡器系列

Si540 数据表

超低抖动任意频率 XO (125 fs), 0.2 至 1500 MHz

Si540 Ultra Series™ 振荡器系列采用 Silicon Laboratories 先进的第四代 DSPLL® 技术, 提供任意输出频率的超低抖动和低相位噪声时钟。这款设备经过出厂前预编程, 可提供频率范围在 0.2 至 1500 MHz 之间的任意频率, 分辨率小于 1 ppb, 可以在整个工作范围内实现整数和小数频率的超低抖动。Si540 振荡器系列提供出色的可靠性、频率稳定性和抗老化性能。片上电源滤波可以实现行业领先的电源噪声抑制特性, 简化了使用开关式电源的噪声系统生成低抖动时钟的任务。Si540 振荡器系列采用行业标准封装, 大幅简化供应链, 使 Silicon Labs 在收到订单后 1-2 周内即可将定制频率样品送达。不同于传统的 XO, Si540 振荡器系列无需使用不同的晶体实现不同的输出频率, 而使用单一晶体和基于 DSPLL IC 的方法提供所需输出频率。这一流程也保证了每个设备的 100% 电气测试。Si540 振荡器系列经工厂配置, 可以满足各种各样的用户规格, 包括频率、输出格式和 OE 引脚位置/极性。特定配置在发货时经过出厂前编程, 消除了与定制频率振荡器有关的长交付周期。

引脚分配



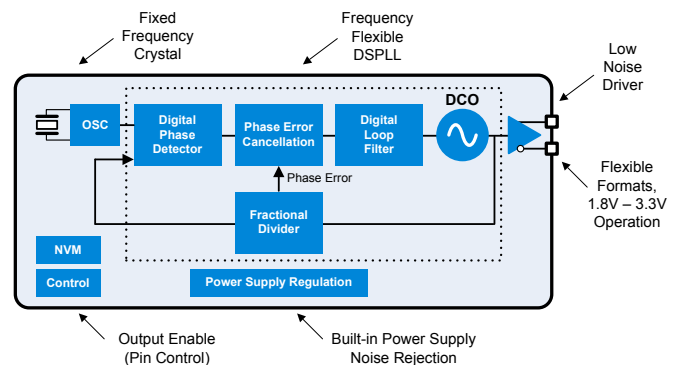
引脚编号	说明
1, 2	订购可选项 OE 表示“输出使能”; NC 表示“无连接”
3	GND 表示“接地”
4	CLK+ 表示“时钟输出”
5	CLK- 表示“互补时钟输出”。CMOS 输出格式下不可用。
6	VDD 表示“电源电压”

主要特点

- 可提供 0.2 至 1500 MHz 之间的任意频率
- 超低抖动: 125 fs RMS (典型值, 12 kHz - 20 MHz)
- 出色的 PSNR 和电源噪声抗扰度: -80 dBc (典型值)
- 7 ppm 稳定性选项 (-40 至 85°C)
- 相同部件编号可实现 3.3 V、2.5 V 和 1.8 V 的供电电压电源操作
- 提供 LVPECL、LVDS、CML、HCSL、CMOS 和双路 CMOS 输出选项
- 2.5×3.2、3.2×5、5×7 mm 封装选项
- 任意定制频率的交付周期都在 1-2 周

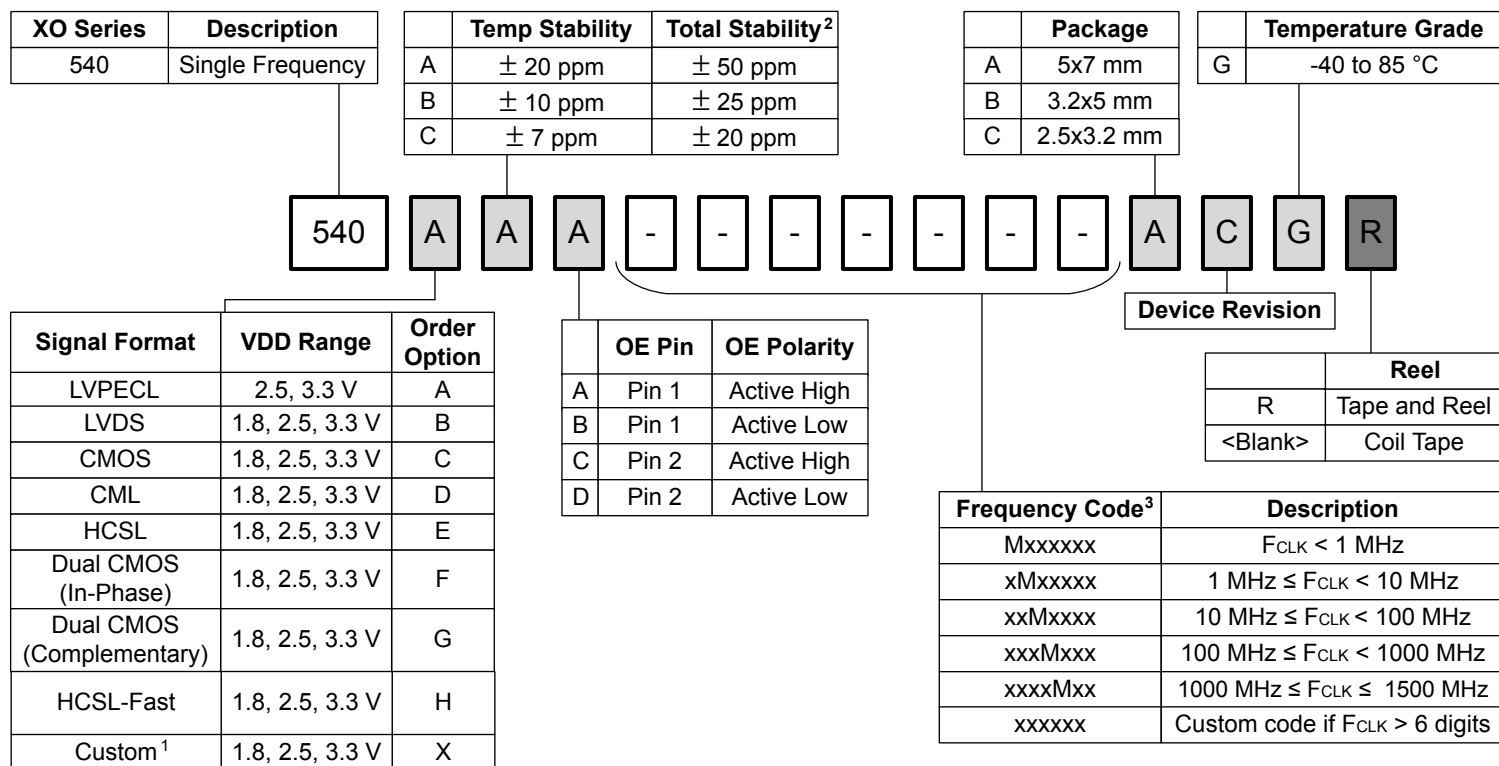
应用

- 100G/200G/400G 相干光学 OTN
- 10G/40G/100G 光以太网
- 3G-SDI/12G-SDI/24G-SDI 广播视频
- 服务器、开关、存储、网卡、搜索加速
- 测试和测量
- 时钟数据恢复
- FPGA/ASIC 时钟设计



1. Ordering Guide

The Si540 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.



Notes:

- Contact Silicon Labs for non-standard configurations.
- Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
- For example: 156.25 MHz = 156M250; 25 MHz = 25M0000. Create custom part numbers at www.silabs.com/oscillators.

1.1 Technical Support

Frequently Asked Questions (FAQ)	www.silabs.com/Si540-FAQ
Oscillator Phase Noise Lookup Utility	www.silabs.com/oscillator-phase-noise-lookup
Quality and Reliability	www.silabs.com/quality
Development Kits	www.silabs.com/oscillator-tools

2. Electrical Specifications

Table 2.1. Electrical Specifications

 $V_{DD} = 1.8\text{ V}, 2.5\text{ or }3.3\text{ V} \pm 5\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		-40	—	85	$^\circ\text{C}$
Frequency Range	F_{CLK}	LVPECL, LVDS, CML	0.2	—	1500	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	V_{DD}	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	I_{DD}	LVPECL (output enabled)	—	100	145	mA
		LVDS/CML (output enabled)	—	75	111	mA
		HCSL (output enabled)	—	80	125	mA
		HCSL-Fast (output enabled)	—	88	137	mA
		CMOS (output enabled)	—	74	108	mA
		Dual CMOS (output enabled)	—	80	125	mA
		Tristate Hi-Z (output disabled)	—	64	100	mA
Temperature Stability		Frequency stability Grade A	-20	—	20	ppm
		Frequency stability Grade B	-10	—	10	ppm
		Frequency stability Grade C	-7	—	7	ppm
Total Stability ¹	F_{STAB}	Frequency stability Grade A	-50	—	50	ppm
		Frequency stability Grade B	-25	—	25	ppm
		Frequency stability Grade C	-20	—	20	ppm
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS ($C_L = 5\text{ pF}$)	—	0.5	1.5	ns
		HCSL, $F_{CLK} > 50\text{ MHz}$	—	—	550	ps
		HCSL-Fast, $F_{CLK} > 50\text{ MHz}$	—	—	275	ps
Duty Cycle	D_C	All formats	45	—	55	%
Output Enable (OE) ²	V_{IH}		$0.7 \times V_{DD}$	—	—	V
	V_{IL}		—	—	$0.3 \times V_{DD}$	V
	T_D	Output Disable Time, $F_{CLK} > 10\text{ MHz}$	—	—	3	μs
	T_E	Output Enable Time, $F_{CLK} > 10\text{ MHz}$	—	—	20	μs
Powerup Time	t_{OSC}	Time from $0.9 \times V_{DD}$ until output frequency (F_{CLK}) within spec	—	—	10	ms

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup VDD Ramp Rate	V_{RAMP}	Fastest V_{DD} ramp rate allowed on startup	—	—	100	V/ms
LVPECL Output Option ³	V_{OC}	Mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	V_O	Swing (diff)	1.1	—	1.9	V_{PP}
LVDS Output Option ⁴	V_{OC}	Mid-level (2.5 V, 3.3 V VDD)	1.125	1.20	1.275	V
		Mid-level (1.8 V VDD)	0.8	0.9	1.0	V
	V_O	Swing ($F_{CLK} \leq 1.4$ GHz)	0.6	0.7	0.9	V_{PP}
		Swing ($F_{CLK} > 1.4$ GHz)	0.5	0.7	0.9	V_{PP}
HCSL Output Option ⁵ HCSL-Fast Output Option ⁵	V_{OH}	Output voltage high	660	750	850	mV
	V_{OL}	Output voltage low	-150	0	150	mV
	V_C	Crossing voltage	250	350	550	mV
CML Output Option (AC-Coupled)	V_O	Swing (diff)	0.6	0.8	1.0	V_{PP}
CMOS Output Option	V_{OH}	$I_{OH} = 8/6/4$ mA for 3.3/2.5/1.8V VDD	$0.85 \times V_{DD}$	—	—	V
	V_{OL}	$I_{OL} = 8/6/4$ mA for 3.3/2.5/1.8V VDD	—	—	$0.15 \times V_{DD}$	V

Notes:

- Total Stability includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 °C.
- OE includes a 50 k Ω pull-up to VDD for OE active high. Includes a 50 k Ω pull-down to GND for OE active low. NC (No Connect) pins include a 50 k Ω pull-down to GND.
- 50 Ω to $V_{DD} - 2.0$ V. Additional DC current from the output driver will flow through the 50 Ω resistors, resulting in a shift in common mode voltage. The measurements in this table have accounted for this.
- $R_{term} = 100$ Ω (differential).
- 50 Ω to GND.

Table 2.2. Clock Output Phase Jitter and PSNR

$V_{DD} = 1.8$ V, 2.5 or 3.3 V \pm 5%, $T_A = -40$ to 85 °C

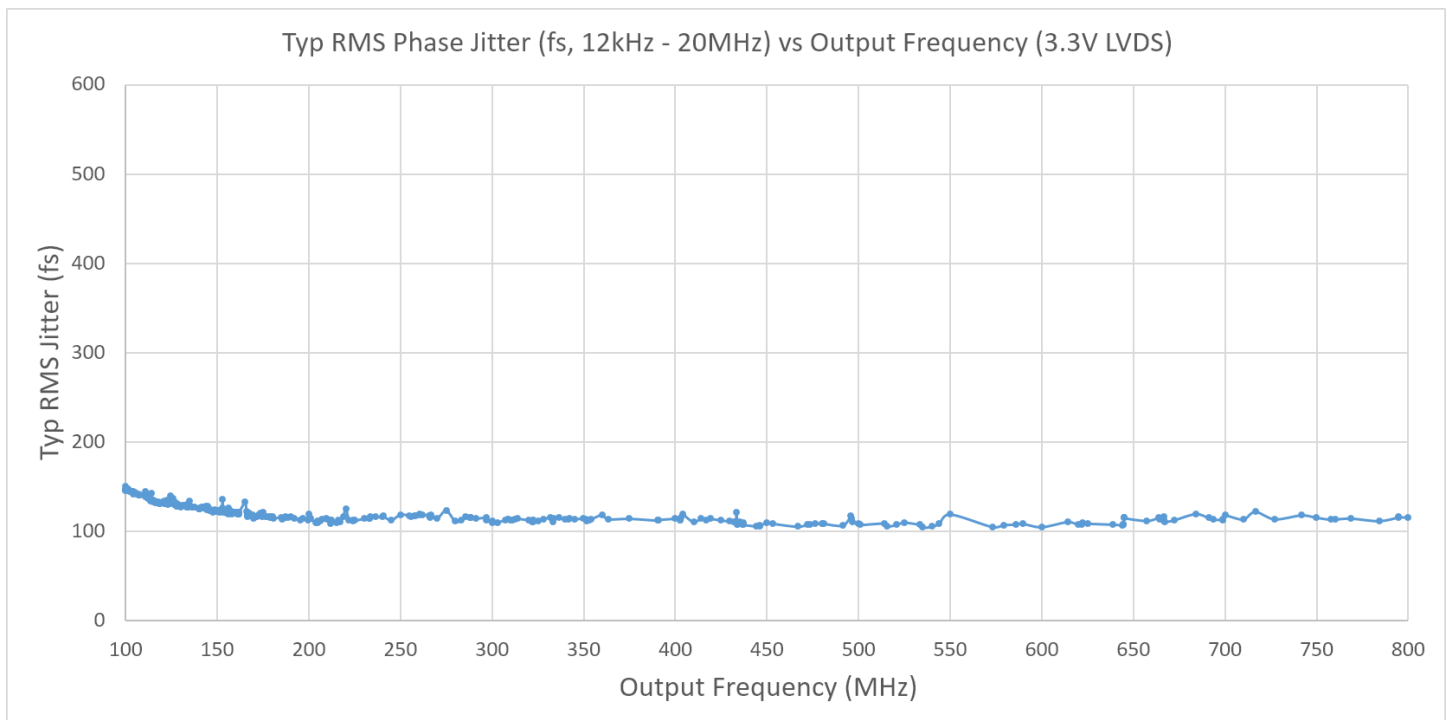
Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12kHz - 20MHz) ¹ 2.5 x 3.2 mm, 3.2 x 5 mm, $F_{CLK} \geq 100$ MHz	ϕ_J	Differential Formats	—	125	200	fs
		CMOS, Dual CMOS	—	200	—	fs
Phase Jitter (RMS, 12kHz - 20MHz) ¹ 5 x 7 mm, $F_{CLK} \geq 100$ MHz	ϕ_J	Differential Formats	—	150	200	fs
		CMOS, Dual CMOS	—	200	—	fs
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output	PSNR	100 kHz sine wave	—	-83	—	dBc
		200 kHz sine wave	—	-83	—	
		500 kHz sine wave	—	-82	—	
		1 MHz sine wave	—	-85	—	

Note:

- Guaranteed by characterization. Jitter inclusive of any spurs.

Table 2.3. 3.2 x 5 mm Clock Output Phase Noise (Typical, 50ppm Total Stability Option)

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-110	-107	-99	dBc/Hz
1 kHz	-121	-120	-109	
10 kHz	-132	-130	-121	
100 kHz	-139	-137	-127	
1 MHz	-151	-149	-138	
10 MHz	-160	-161	-155	
20 MHz	-161	-162	-157	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	-113	-110	-100	dBc/Hz
1 kHz	-123	-120	-110	
10 kHz	-133	-130	-119	
100 kHz	-139	-137	-127	
1 MHz	-151	-149	-138	
10 MHz	-162	-166	-156	
20 MHz	-163	-167	-157	



Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

Figure 2.1. Phase Jitter vs. Output Frequency

Table 2.4. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL): 3.2 x 5, 5 x 7 packages	1
Moisture Sensitivity Level (MSL): 2.5 x 3.2 package	2
Contact Pads: 3.2x5, 5x7 packages	Au/Ni (0.3 - 1.0 μm / 1.27 - 8.89 μm)
Contact Pads: 2.5x3.2 packages	Au/Pd/Ni (0.03 - 0.12 μm / 0.1 - 0.2 μm / 3.0 - 8.0 μm)
Note:	
1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx .	

Table 2.5. Thermal Conditions

Max Junction Temperature = 125° C

Package	Parameter	Symbol	Test Condition	Value	Unit
2.5 x 3.2 mm 6-pin DFN	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air, 85 °C	80	°C/W
	Thermal Parameter Junction to Board	Ψ_{JB}	Still Air, 85 °C	39	°C/W
	Thermal Parameter Junction to Top Center	Ψ_{JT}	Still Air, 85 °C	17	°C/W
3.2 x 5 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air, 85 °C	55	°C/W
	Thermal Parameter Junction to Board	Ψ_{JB}	Still Air, 85 °C	20	°C/W
	Thermal Parameter Junction to Top Center	Ψ_{JT}	Still Air, 85 °C	20	°C/W
5 x 7 mm 6-pin CLCC	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air, 85 °C	53	°C/W
	Thermal Parameter Junction to Board	Ψ_{JB}	Still Air, 85 °C	26	°C/W
	Thermal Parameter Junction to Top Center	Ψ_{JT}	Still Air, 85 °C	26	°C/W
Note:					
1. Based on PCB Dimensions: 4.5" x 7", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.					

Table 2.6. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	T_{AMAX}	95	°C
Storage Temperature	T_S	–55 to 125	°C
Supply Voltage	V_{DD}	–0.5 to 3.8	°C
Input Voltage	V_{IN}	–0.5 to $V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature ²	T_{PEAK}	260	°C
Solder Time at T_{PEAK} ²	T_P	20–40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple XOs with a single Si540 device.

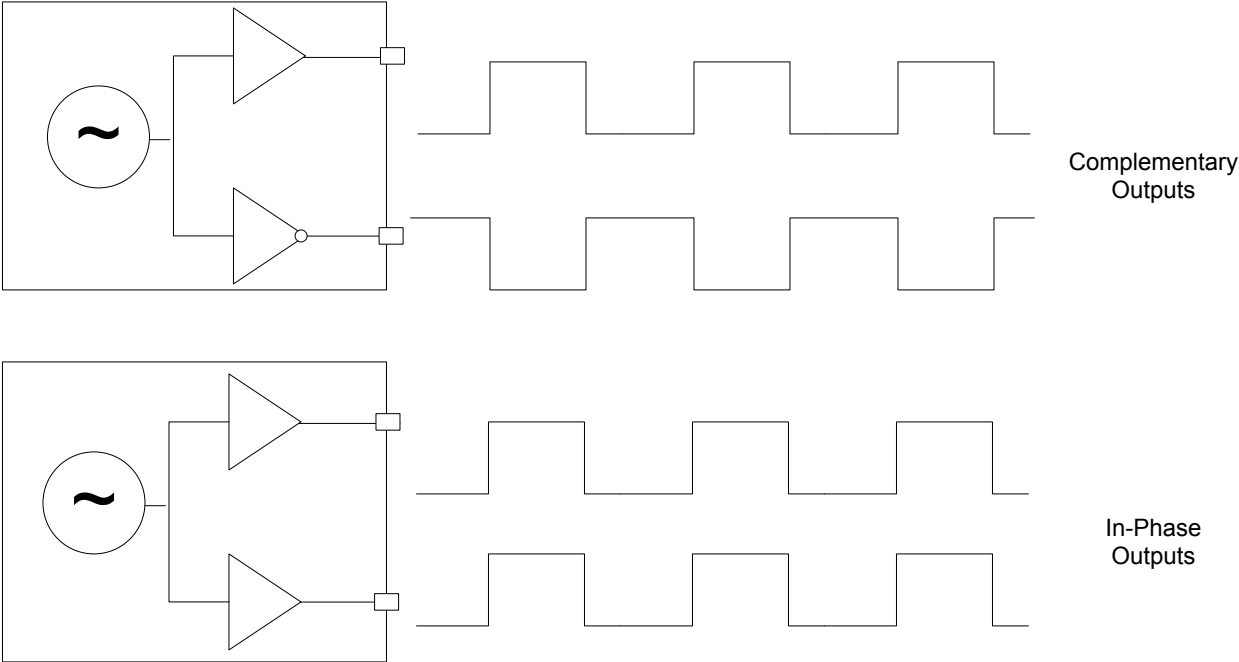


Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

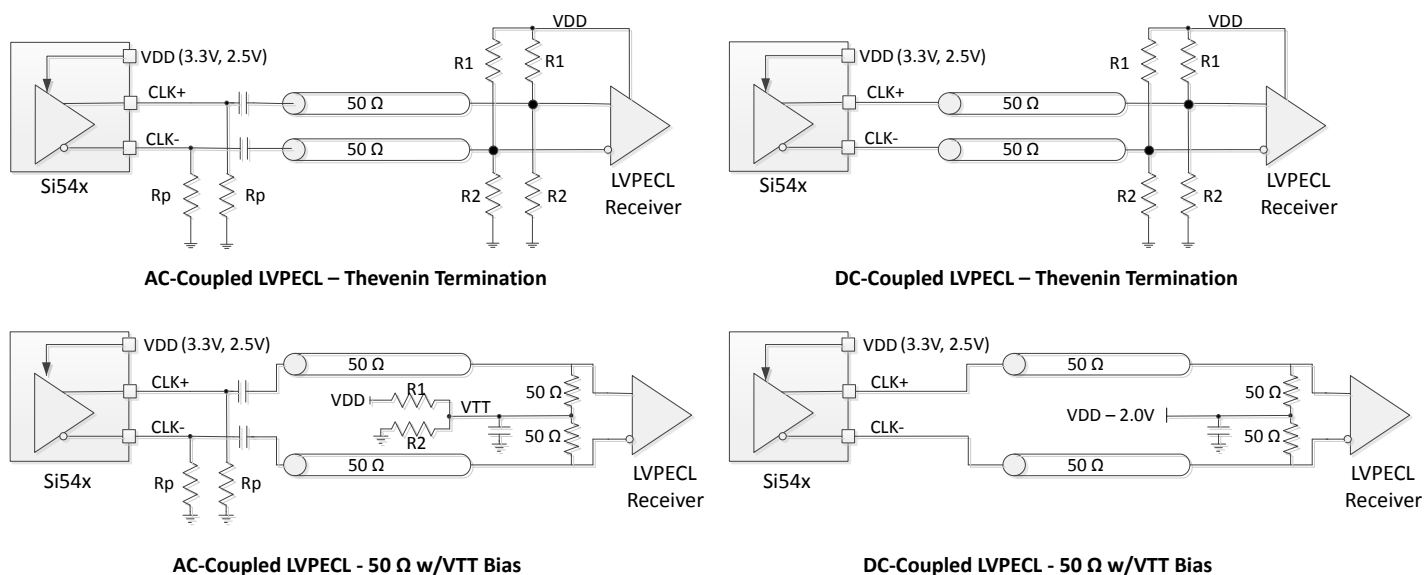


Figure 4.1. LVPECL Output Terminations

AC Coupled LVPECL Termination Resistor Values				DC Coupled LVPECL Termination Resistor Values		
VDD	R1	R2	Rp	VDD	R1	R2
3.3 V	82.5 Ω	127 Ω	130 Ω	3.3 V	127 Ω	82.5 Ω
2.5 V	62.5 Ω	250 Ω	90 Ω	2.5 V	250 Ω	62.5 Ω

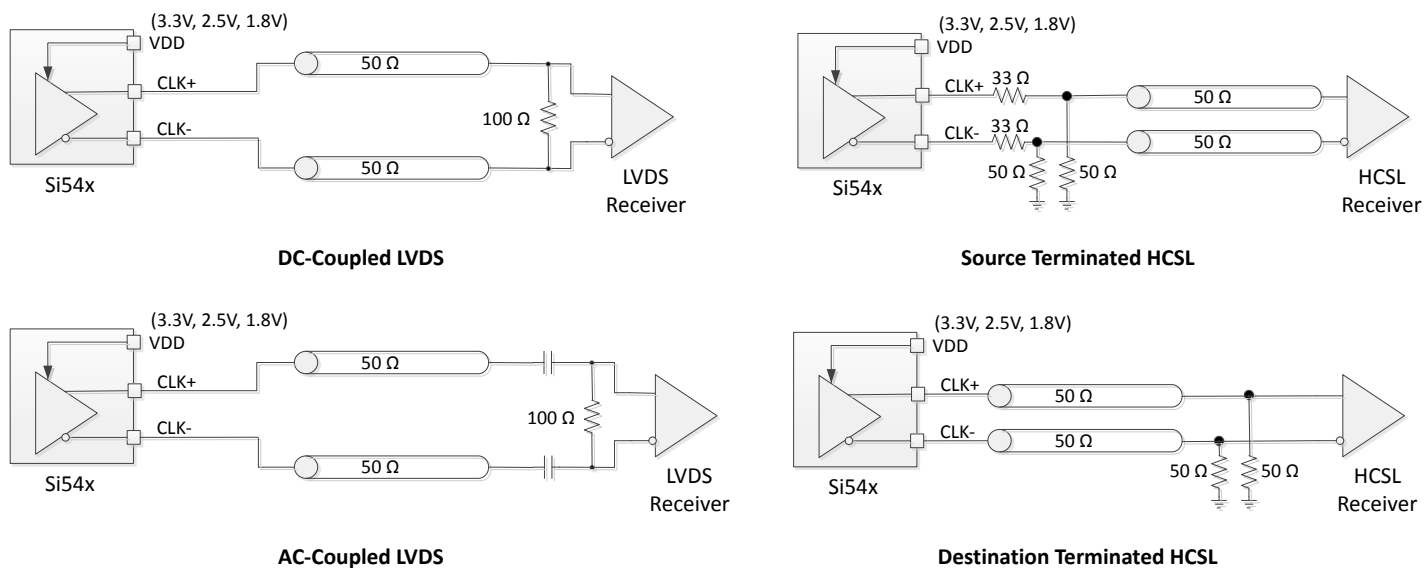


Figure 4.2. LVDS and HCSL Output Terminations

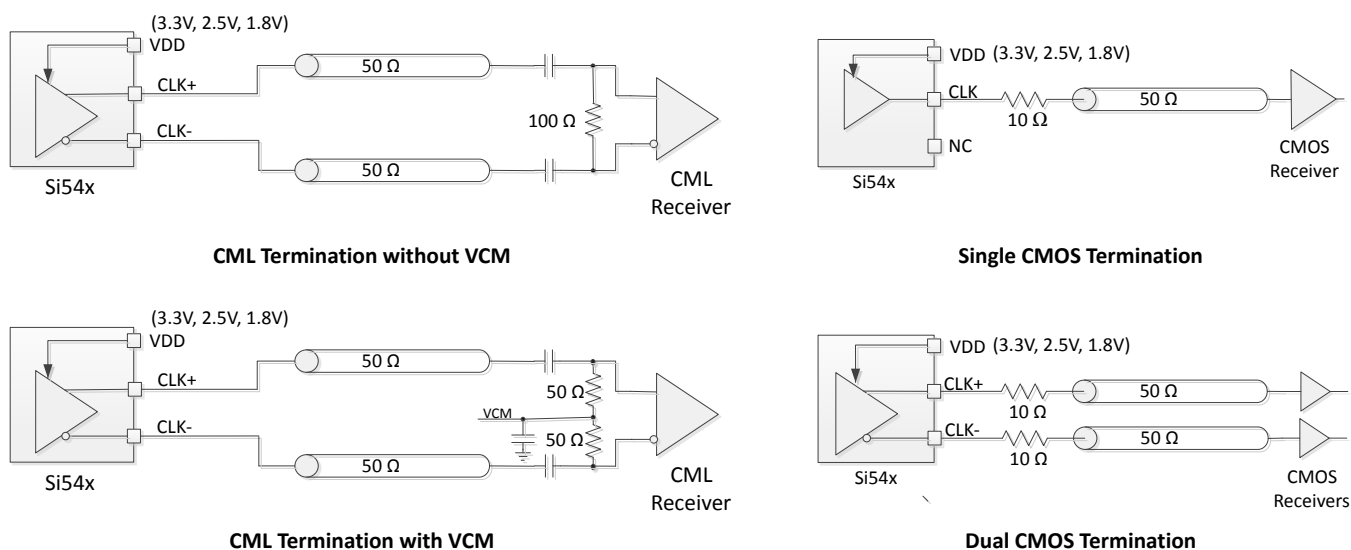


Figure 4.3. CML and CMOS Output Terminations

5. Package Outline

5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si540. The table below lists the values for the dimensions shown in the illustration.

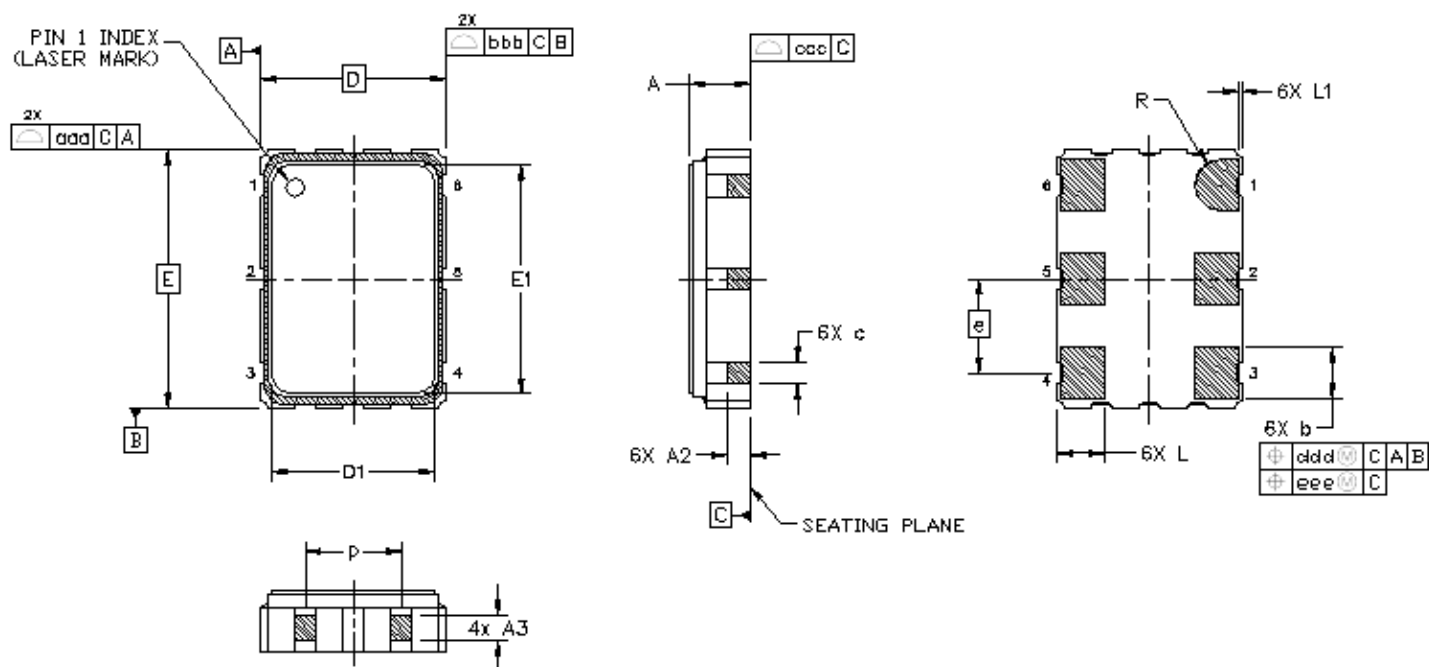


Figure 5.1. Si540 (5×7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.13	1.28	1.43	L	1.17	1.27	1.37
A2	0.50	0.55	0.60	L1	0.05	0.10	0.15
A3	0.50	0.55	0.60	p	1.70	—	1.90
b	1.30	1.40	1.50	R	0.70 REF		
c	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.30	4.40	4.50	ccc	0.08		
e	2.54 BSC			ddd	0.10		
E	7.00 BSC			eee	0.05		
E1	6.10	6.20	6.30				

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si540. The table below lists the values for the dimensions shown in the illustration.

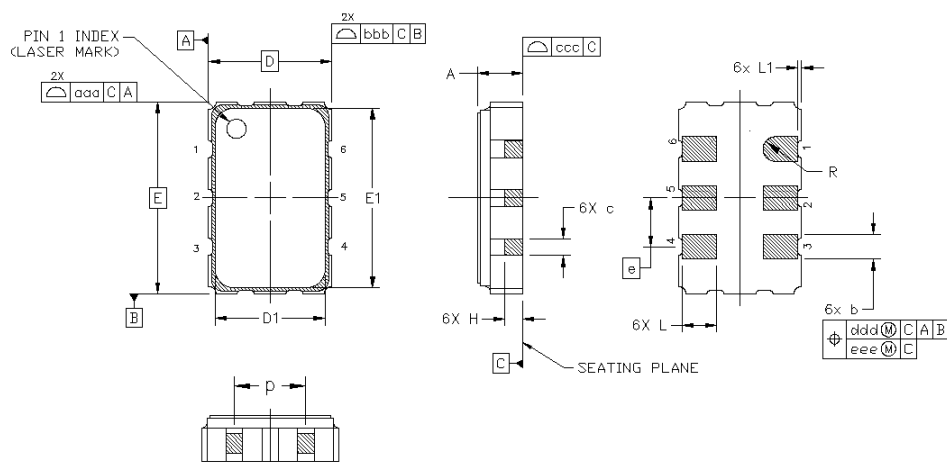


Figure 5.2. Si540 (3.2×5 mm) Outline Diagram

Table 5.2. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.06	1.17	1.33
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D	3.20 BSC		
D1	2.55	2.60	2.65
e	1.27 BSC		
E	5.00 BSC		
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.80	0.90	1.00
L1	0.05	0.10	0.15
p	1.36	1.46	1.56
R	0.32 REF		
aaa	0.15		
bbb	0.15		
ccc	0.08		
ddd	0.10		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.3 Package Outline (2.5x3.2 mm)

The figure below illustrates the package details for the 2.5x3.2 mm Si540. The table below lists the values for the dimensions shown in the illustration.

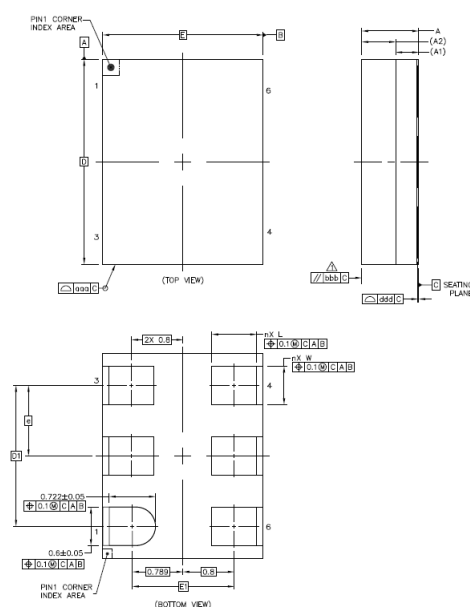


Figure 5.3. Si540 (2.5x3.2 mm) Outline Diagram

Table 5.3. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	0.90	0.95	1.00
A1		0.36 REF	
A2		0.53 REF	
W	0.55	0.60	0.65
D		3.2 BSC	
E		2.5 BSC	
e		1.10 BSC	
L	0.65	0.70	0.75
n		5	
D1		2.2 BSC	
E1		1.589 BSC	
aaa		0.10	
bbb		0.10	
ddd		0.08	

Notes:

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6. PCB Land Pattern

6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.

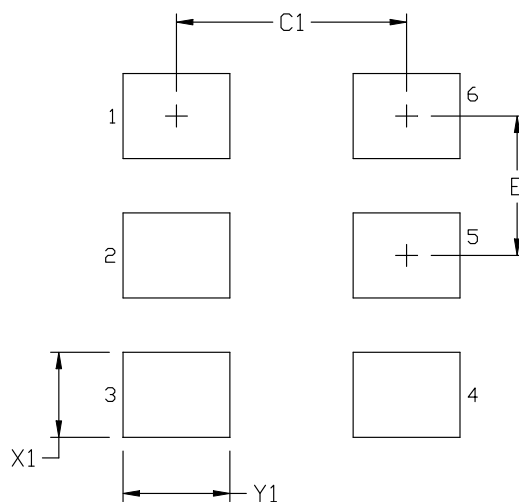


Figure 6.1. Si540 (5×7 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.

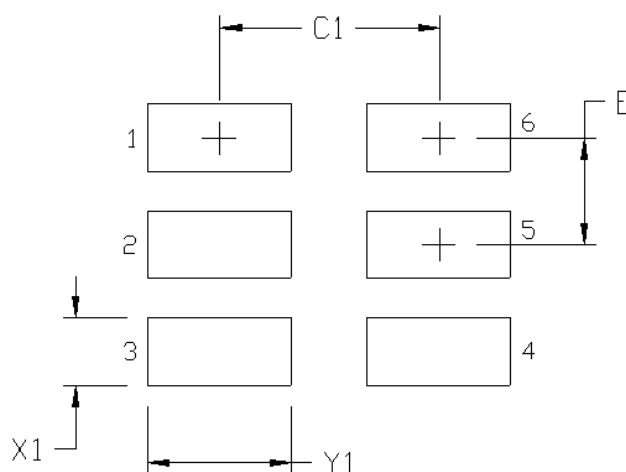


Figure 6.2. Si540 (3.2×5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3 PCB Land Pattern (2.5×3.2 mm)

The figure below illustrates the 2.5×3.2 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.

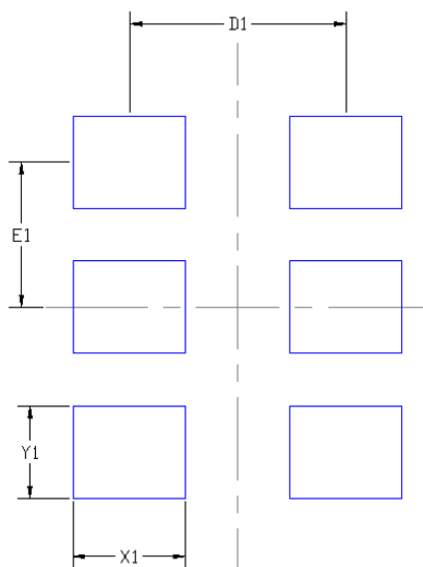


Figure 6.3. Si540 (2.5×3.2 mm) PCB Land Pattern

Table 6.3. PCB Land Pattern Dimensions (mm)

Dimension	Description	Value (mm)
X1	Width - leads on long sides	0.85
Y1	Height - leads on long sides	0.7
D1	Pitch in X directions of XLY1 leads	1.639
E1	Lead pitch XLY1 leads	1.10

Notes: The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Marking (5x7 and 3.2x5 Packages)

The figure below illustrates the mark specification for the Si540 5x7 and 3.2x5 package sizes. The table below lists the line information.

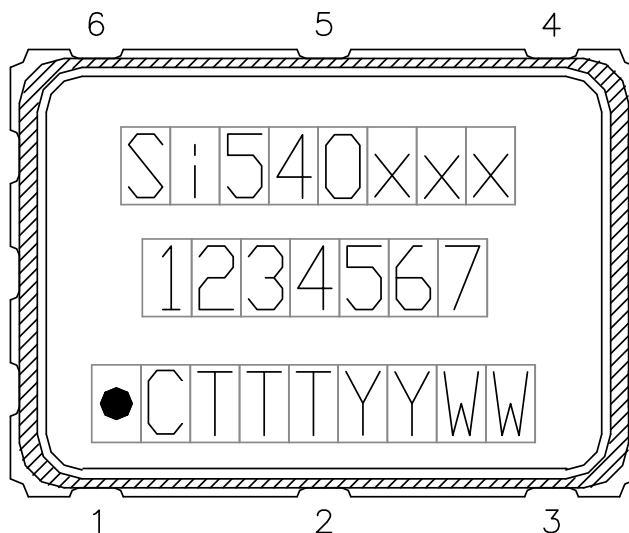


Figure 7.1. Mark Specification

Table 7.1. Si540 Top Mark Description

Line	Position	Description
1	1–8	"Si540", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si540AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (C)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

8. Top Marking (2.5x3.2 Package)

The figure below illustrates the mark specification for the Si540 2.5x3.2 package sizes. The table below lists the line information.

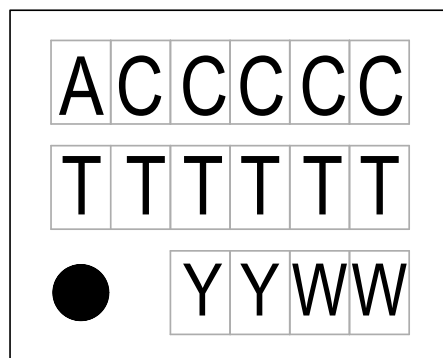


Figure 8.1. Mark Specification

Table 8.1. Si540 Top Mark Description

Line	Position	Description
1	1–6	A = Si540, CCCCC = Custom Mark Code
2	Trace Code	
	1–6	Six-digit trace code per assembly release instructions
3	Position 1	Pin 1 orientation mark (dot)
	Position 2–3	Year (last two digits of the year), to be assigned by assembly site (exp: 2017 = 17)
	Position 4–5	Calendar Work Week number (1–53), to be assigned by assembly site

9. Revision History

Revision 1.3

June 2021

- Updated Ordering Guide and Topmark for Rev. C silicon
- Added HCSL-Fast (faster t_R/t_F) ordering option
- Updated Table 2.1, Powerup VDD Ramp Rate

Revision 1.2

September 2020

- Updated Table 2.1, Powerup VDD Ramp Rate and LVDS Swing

Revision 1.1

November 2019

- Added 2.5x3.2 mm package option

Revision 1.0

July 2018

- Added 20 ppm total stability option.

Revision 0.75

March, 2018

- Added 25 ppm total stability option.

Revision 0.71

December 11, 2017

- Added 5x7 package and land pattern.

Revision 0.7

June 27, 2017

- Initial release.

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows.

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support & Community
www.silabs.com/community

Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

Note: This content may contain offensive terminology that is now obsolete. Silicon Labs is replacing these terms with inclusive language wherever possible. For more information, visit www.silabs.com/about-us/inclusive-lexicon-project

Trademark Information

Silicon Laboratories Inc., Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR®, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com