

KVR667D2D4F5/4GI
4GB 512M x 72-Bit PC2-5300
CL5 ECC 240-Pin FBDIMM

Description:

This document describes ValueRAM's 4GB (512M x 72-bit) PC2-5300 CL5 SDRAM (Synchronous DRAM) fully buffered ECC "dual rank" "Intel Certified" memory module. This module is based on eighteen stacked 512M x 4-bit (thirty-six 256M x 4-bit) 667MHz DDR2 FBGA components. The module also includes an AMB device (Advanced Memory Buffer). The electrical and mechanical specifications are as follows:

Feature:

- FBDIMM Module: 240-pin
- JEDEC Standard: R/C H or E
- Memory Organization: 2 rank of x4 devices
- DDR2 DRAM Interface: SSTL_18
- DDR2 Speed Grade: 667 Mbps
- CAS Latency: 5-5-5
- Module Bandwidth: 5.3 GB/s
- DRAM: VDD = VDDQ = 1.8V
- AMB: VCC = VCCFBD = 1.5V
- EEPROM: VDDSPD = 3.3V (typical)
- Heat Spreader: Full DIMM Heat Spreader (FDHS)
- PCB Height: 30.35mm, double-side
- RoHS Compliant

DDR2 240-pin FBDIMM Pinout:

| Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side | Pin # | Front Side | Pin # | Back Side |
|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|-------|-----------------|
| 1 | V _{DD} | 121 | V _{DD} | 31 | PN3 | 151 | SN3 | 61 | PN9 | 181 | SN9 | 91 | PS9 | 211 | SS9 |
| 2 | V _{DD} | 122 | V _{DD} | 32 | PN3 | 152 | SN3 | 62 | V _{SS} | 182 | V _{SS} | 92 | V _{SS} | 212 | V _{SS} |
| 3 | V _{DD} | 123 | V _{DD} | 33 | V _{SS} | 153 | V _{SS} | 63 | PN10 | 183 | SN10 | 93 | PS5 | 213 | SS5 |
| 4 | V _{SS} | 124 | V _{SS} | 34 | PN4 | 154 | SN4 | 64 | PN10 | 184 | SN10 | 94 | PS5 | 214 | SS5 |
| 5 | V _{DD} | 125 | V _{DD} | 35 | PN4 | 155 | SN4 | 65 | V _{SS} | 185 | V _{SS} | 95 | V _{SS} | 215 | V _{SS} |
| 6 | V _{DD} | 126 | V _{DD} | 36 | V _{SS} | 156 | V _{SS} | 66 | PN11 | 186 | SN11 | 96 | PS6 | 216 | SS6 |
| 7 | V _{DD} | 127 | V _{DD} | 37 | PN5 | 157 | SN5 | 67 | PN11 | 187 | SN11 | 97 | PS6 | 217 | SS6 |
| 8 | V _{SS} | 128 | V _{SS} | 38 | PN5 | 158 | SN5 | 68 | V _{SS} | 188 | V _{SS} | 98 | V _{SS} | 218 | V _{SS} |
| 9 | V _{CC} | 129 | V _{CC} | 39 | V _{SS} | 159 | V _{SS} | KEY | | | | 99 | PS7 | 219 | SS7 |
| 10 | V _{CC} | 130 | V _{CC} | 40 | PN13 | 160 | SN13 | 69 | V _{SS} | 189 | V _{SS} | 100 | PS7 | 220 | SS7 |
| 11 | V _{SS} | 131 | V _{SS} | 41 | PN13 | 161 | SN13 | 70 | PS0 | 190 | SS0 | 101 | V _{SS} | 221 | V _{SS} |
| 12 | V _{CC} | 132 | V _{CC} | 42 | V _{SS} | 162 | V _{SS} | 71 | PS0 | 191 | SS0 | 102 | PS8 | 222 | SS8 |
| 13 | V _{CC} | 133 | V _{CC} | 43 | V _{SS} | 163 | V _{SS} | 72 | V _{SS} | 192 | V _{SS} | 103 | PS8 | 223 | SS8 |
| 14 | V _{SS} | 134 | V _{SS} | 44 | RFU* | 164 | RFU* | 73 | PS1 | 193 | SS1 | 104 | V _{SS} | 224 | V _{SS} |
| 15 | V _{TT} | 135 | V _{TT} | 45 | RFU* | 165 | RFU* | 74 | PS1 | 194 | SS1 | 105 | RFU** | 225 | RFU** |
| 16 | VID1 | 136 | VID0 | 46 | V _{SS} | 166 | V _{SS} | 75 | V _{SS} | 195 | V _{SS} | 106 | RFU** | 226 | RFU** |
| 17 | RESET | 137 | DNU/M_Test | 47 | V _{SS} | 167 | V _{SS} | 76 | PS2 | 196 | SS2 | 107 | V _{SS} | 227 | V _{SS} |
| 18 | V _{SS} | 138 | V _{SS} | 48 | PN12 | 168 | SN12 | 77 | PS2 | 197 | SS2 | 108 | V _{DD} | 228 | SCK |
| 19 | RFU** | 139 | RFU** | 49 | PN12 | 169 | SN12 | 78 | V _{SS} | 198 | V _{SS} | 109 | V _{DD} | 229 | SCK |
| 20 | RFU** | 140 | RFU** | 50 | V _{SS} | 170 | V _{SS} | 79 | PS3 | 199 | SS3 | 110 | V _{SS} | 230 | V _{SS} |
| 21 | V _{SS} | 141 | V _{SS} | 51 | PN6 | 171 | SN6 | 80 | PS3 | 200 | SS3 | 111 | V _{DD} | 231 | V _{DD} |
| 22 | PN0 | 142 | SN0 | 52 | PN6 | 172 | SN6 | 81 | V _{SS} | 201 | V _{SS} | 112 | V _{DD} | 232 | V _{DD} |
| 23 | PN0 | 143 | SN0 | 53 | V _{SS} | 173 | V _{SS} | 82 | PS4 | 202 | SS4 | 113 | V _{DD} | 233 | V _{DD} |
| 24 | V _{SS} | 144 | V _{SS} | 54 | PN7 | 174 | SN7 | 83 | PS4 | 203 | SS4 | 114 | V _{SS} | 234 | V _{SS} |
| 25 | PN1 | 145 | SN1 | 55 | PN7 | 175 | SN7 | 84 | V _{SS} | 204 | V _{SS} | 115 | V _{DD} | 235 | V _{DD} |
| 26 | PN1 | 146 | SN1 | 56 | V _{SS} | 176 | V _{SS} | 85 | V _{SS} | 205 | V _{SS} | 116 | V _{DD} | 236 | V _{DD} |
| 27 | V _{SS} | 147 | V _{SS} | 57 | PN8 | 177 | SN8 | 86 | RFU* | 206 | RFU* | 117 | V _{TT} | 237 | V _{TT} |
| 28 | PN2 | 148 | SN2 | 58 | PN8 | 178 | SN8 | 87 | RFU* | 207 | RFU* | 118 | SA2 | 238 | VDDSPD |
| 29 | PN2 | 149 | SN2 | 59 | V _{SS} | 179 | V _{SS} | 88 | V _{SS} | 208 | V _{SS} | 119 | SDA | 239 | SA0 |
| 30 | V _{SS} | 150 | V _{SS} | 60 | PN9 | 180 | SN9 | 89 | V _{SS} | 209 | V _{SS} | 120 | SCL | 240 | SA1 |
| | | | | | | | | 90 | PS9 | 210 | SS9 | | | | |

RFU = Reserved Future Use.

* These pin positions are reserved for forwarded clocks to be used in future module implementations

** These pin positions are reserved for future architecture flexibility

1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/PN12, SN12/SN12, PN13/PN13, SN13/SN13, PS9/PS9, SS9/SS9

DIMM Connector Pin Description:

| Pin Name | Pin Description | Count |
|-------------------------------|---|-------|
| SCK | System Clock Input, positive line ¹ | 1 |
| $\overline{\text{SCK}}$ | System Clock Input, negative line ¹ | 1 |
| PN[13:0] | Primary Northbound Data, positive lines | 14 |
| $\overline{\text{PN}}$ [13:0] | Primary Northbound Data, negative lines | 14 |
| PS[9:0] | Primary Southbound Data, positive lines | 10 |
| $\overline{\text{PS}}$ [9:0] | Primary Southbound Data, negative lines | 10 |
| SN[13:0] | Secondary Northbound Data, positive lines | 14 |
| $\overline{\text{SN}}$ [13:0] | Secondary Northbound Data, negative lines | 14 |
| SS[9:0] | Secondary Southbound Data, positive lines | 10 |
| $\overline{\text{SS}}$ [9:0] | Secondary Southbound Data, negative lines | 10 |
| SCL | Serial Presence Detect (SPD) Clock Input | 1 |
| SDA | SPD Data Input / Output | 1 |
| SA[2:0] | SPD Address Inputs, also used to select the DIMM number in the AMB | 3 |
| VID[1:0] | Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V | 2 |
| $\overline{\text{RESET}}$ | AMB reset signal | 1 |
| RFU | Reserved for Future Use ² | 16 |
| V_{CC} | AMB Core Power and AMB Channel Interface Power (1.5 Volt) | 8 |
| V_{DD} | DRAM Power and AMB DRAM I/O Power (1.8 Volt) | 24 |
| V_{TT} | DRAM Address/Command/Clock Termination Power ($V_{DD}/2$) | 4 |
| V_{DDSPD} | SPD Power | 1 |
| V_{SS} | Ground | 80 |
| DNU/M_Test | The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of V_{ref} which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time. 1 | 1 |
| Total | | 240 |

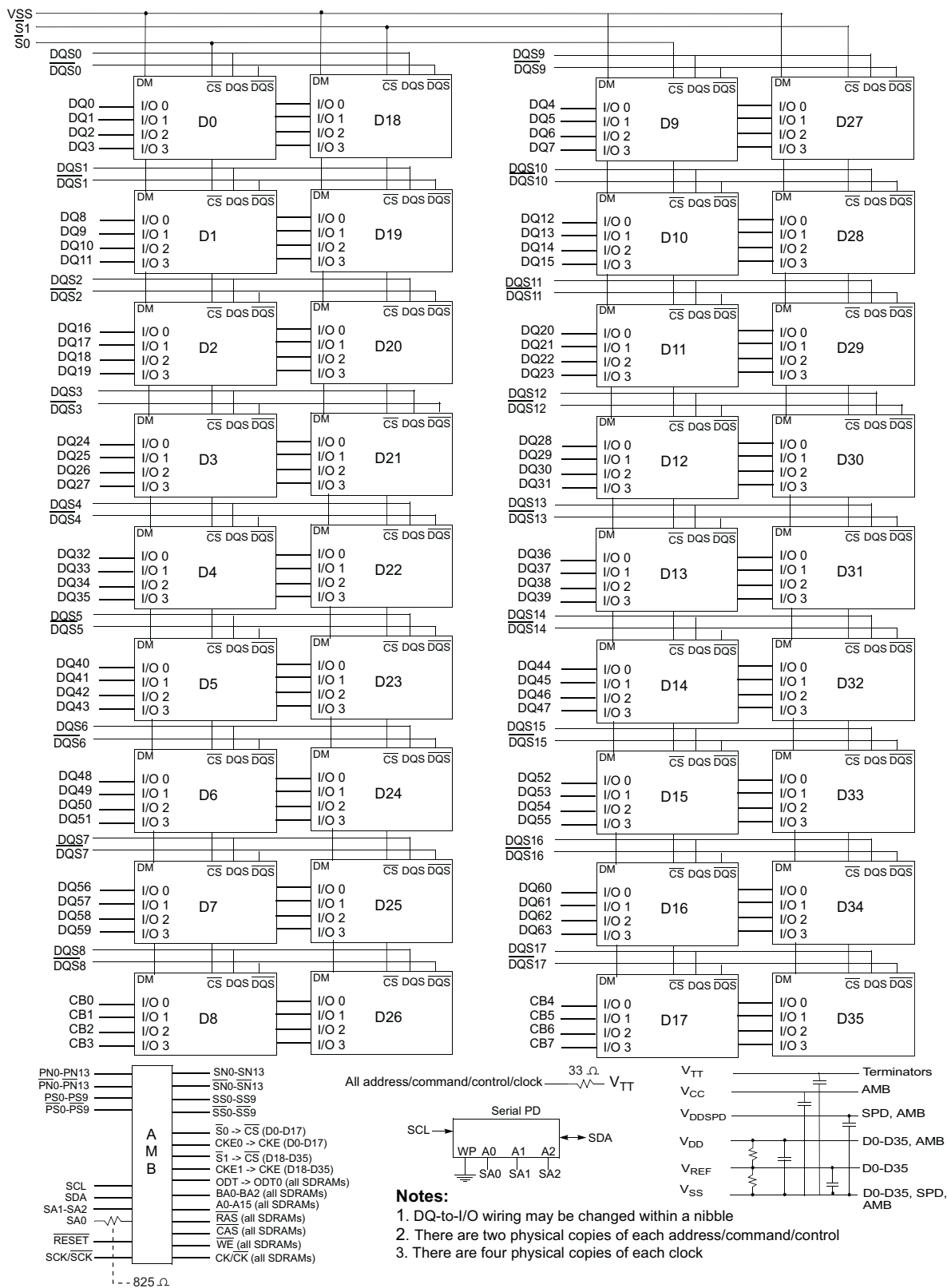
1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/ $\overline{\text{CK}}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

Absolute Maximum Ratings

| Symbol | Parameter | MIN | MAX | Units |
|-------------------|---|------|-------------------|-------|
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.3 | 1.75 | V |
| V_{CC} | Voltage on V_{CC} pin relative to V_{SS} | -0.3 | 1.75 | V |
| V_{DD} | Voltage V_{DD} pin relative to V_{SS} | -0.5 | 2.3 | V |
| V_{TT} | Voltage on V_{TT} pin relative to V_{SS} | -0.5 | 2.3 | V |
| T_{STG} | Storage temperature | -55 | 100 | °C |
| T_{CASE} | DDR2 SDRAM device operating temperature (Ambient) | 0 | 95 ⁽¹⁾ | °C |
| | AMB device operating temperature (Ambient) | 0 | 110 | °C |

Note: (1) Above 85°C DRAM case temperature the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$.

Functional Block Diagram:



Architecture:

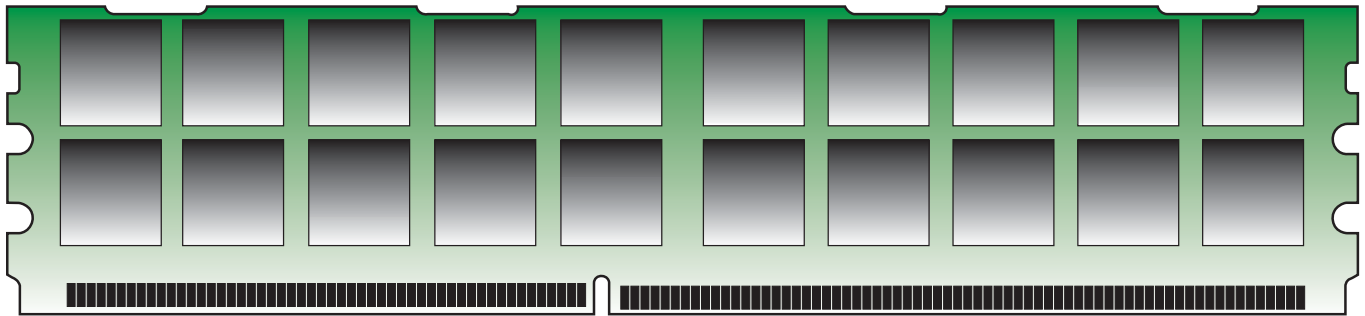
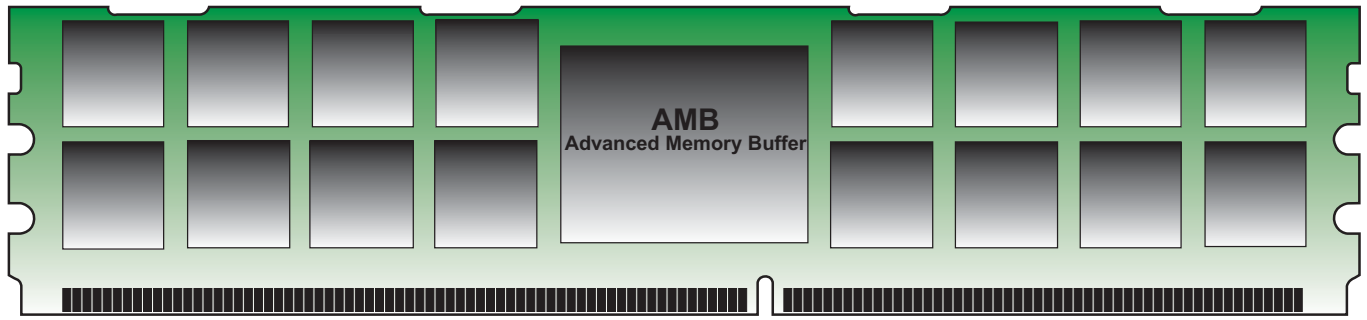
Advanced Memory Buffer Pin Description:

| Pin Name | Pin Description | Count |
|--|---|------------|
| FB-DIMM Channel Signals | | 99 |
| SCK | System Clock Input, positive line | 1 |
| $\overline{\text{SCK}}$ | System Clock Input, negative line | 1 |
| PN[13:0] | Primary Northbound Data, positive lines | 14 |
| $\overline{\text{PN}}$ [13:0] | Primary Northbound Data, negative lines | 14 |
| PS[9:0] | Primary Southbound Data, positive lines | 10 |
| $\overline{\text{PS}}$ [9:0] | Primary Southbound Data, negative lines | 10 |
| SN[13:0] | Secondary Northbound Data, positive lines | 14 |
| $\overline{\text{SN}}$ [13:0] | Secondary Northbound Data, negative lines | 14 |
| SS[9:0] | Secondary Southbound Data, positive lines | 10 |
| $\overline{\text{SS}}$ [9:0] | Secondary Southbound Data, negative lines | 10 |
| FBDRES | To an external precision calibration resistor connected to Vcc | 1 |
| DDR2 Interface Signals | | 175 |
| DQS[8:0] | Data Strobes, positive lines | 9 |
| $\overline{\text{DQS}}$ [8:0] | Data Strobes, negative lines | 9 |
| DQS[17:9]/DM[8:0] | Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes. | 9 |
| $\overline{\text{DQS}}$ [17:9] | Data Strobes (x4 DRAM only), negative lines | 9 |
| DQ[63:0] | Data | 64 |
| CB[7:0] | Checkbits | 8 |
| A[15:0]A, A[15:0]B | Addresses. A10 is part of the pre-charge command | 32 |
| BA[2:0]A, BA[2:0]B | Bank Addresses | 6 |
| $\overline{\text{RASA}}$, $\overline{\text{RASB}}$ | Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$ [1:0]. | 2 |
| $\overline{\text{CASA}}$, $\overline{\text{CASB}}$ | Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$ [1:0]. | 2 |
| $\overline{\text{WEA}}$, $\overline{\text{WEB}}$ | Part of command, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CS}}$ [1:0]. | 2 |
| ODTA, ODTB | On-die Termination Enable | 2 |
| CKE[1:0]A, CKE[1:0]B | Clock Enable (one per rank) | 4 |
| $\overline{\text{CS}}$ [1:0]A, $\overline{\text{CS}}$ [1:0]B | Chip Select (one per rank) | 4 |
| CLK[3:0] | CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use. | 4 |
| $\overline{\text{CLK}}$ [3:0] | Negative lines for CLK[3:0] | 4 |
| DDRC_C14 | DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18. | 1 |
| DDRC_B18 | DDR Compensation: Resistor connected to common return pin DDRC_C14 | 1 |
| DDRC_C18 | DDR Compensation: Resistor connected to common return pin DDRC_C14 | 1 |
| DDRC_B12 | DDR Compensation: Resistor connected to V _{SS} | 1 |
| DDRC_C12 | DDR Compensation: Resistor connected to V _{DD} | 1 |

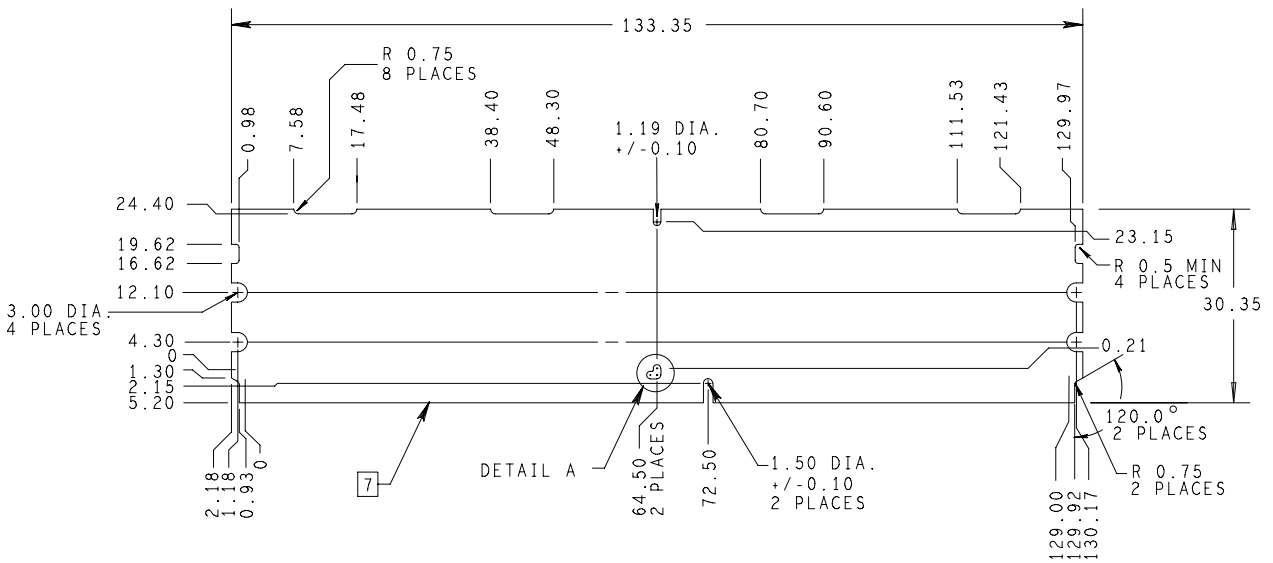
Advanced Memory Buffer Pin Description:

| SPD Bus Interface Signals | | 5 |
|---|--|------------|
| SCL | Serial Presence Detect (SPD) Clock Input | 1 |
| SDA | SPD Data Input / Output | 1 |
| SA[2:0] | SPD Address Inputs, also used to select the DIMM number in the AMB | 3 |
| Miscellaneous Signals | | 163 |
| PLLTSTO | PLL Clock Observability Output | 1 |
| VCCAPLL | Analog VCC for the PLL. Tied with low pass filter to VCC. | 1 |
| VSSAPLL | Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM. | 1 |
| TEST_pin# | Leave floating on the DIMM | 6 |
| TESTLO_pin# | Tie to ground on the DIMM ² | 5 |
| BFUNC | Tie to ground to set functionality as "buffer on DIMM." | 1 |
| $\overline{\text{RESET}}$ | AMB reset signal | 1 |
| NC | No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands. | 129 |
| RFU | Reserved for Future Use | 18 |
| Power/Ground Signals | | 213 |
| V _{CC} | AMB Core Power (1.5 Volt) | 24 |
| V _{CCFBD} | AMB Channel I/O Power (1.5 Volt) | 8 |
| V _{DD} | AMB DRAM I/O Power (1.8 Volt) | 24 |
| V _{DDSPD} | SPD Power (3.3 Volt) | 1 |
| V _{SS} | Ground | 156 |
| Total | | 655 |
| <p>1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/$\overline{\text{CK}}$ frequency.</p> <p>2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.</p> | | |

Package Dimensions:



(Units = millimeters)



Units: inches (millimeters)

