PRIMARY CONTROL (PC PIN)

Module Enable / Disable. The module can be disabled by pulling the PC below 2.3 V with respect to the –Input. This should be done with an open-collector transistor, relay, or optocoupler. Multiple converters may be disabled with a single transistor or relay via "ORing" diodes. When using a mechanical switch or relay to control the PC pin, please ensure that the contacts are properly debounced with a capacitor (10 nF max.) to avoid switch bounce.

An optocoupler must be used when converters are located on different PC boards, when a common-mode inductor is used directly at the module input, or when the distance between the converters would cause excessive voltage drops. Under no circumstances should the PC pin be pulled negative more than a diode drop below the module –IN. (Figure 2–1) When the PC pin is pulled low the PC current will pulse similar to the PC voltage shown in Figure 2–4. When the outputs of two or more converters are connected in a parallel array to increase system power the converters should be "group enabled" to ensure that all the converters start at the same time. The PC pins of all converters in the array should be controlled by an external circuit which will enable the converters once the input voltage is within the normal operating range.

Primary Auxiliary Supply. At 5.75 V, the PC can source up to 1.5 mA. In the example shown in Figure 2–3, PC powers a LED to indicate the module is enabled. Another example of an isolated on-state indicator is shown in Figure 2–5.

NOTE: When the module has detected a fault or when the input voltage is above or below the normal operating range the PC voltage will pulse.

Module Alarm. The module contains "watchdog" circuitry that monitors input voltage, operating temperature, and internal operating parameters. (Figures 2–2a and 2–2b) If any of these parameters is outside their allowable operating range, the module will shut down and PC will go low. (Figure 2–4) Then PC will periodically go high and the module will check to see if the fault (as an example, input undervoltage) has cleared. If the fault has not been cleared, PC will go low again and the cycle will restart. The SC pin will go low when a fault occurs and return to its normal state after the fault has been cleared. An example of using a comparator for monitoring on the secondary is shown in Figures 2–6a and 2–6b.

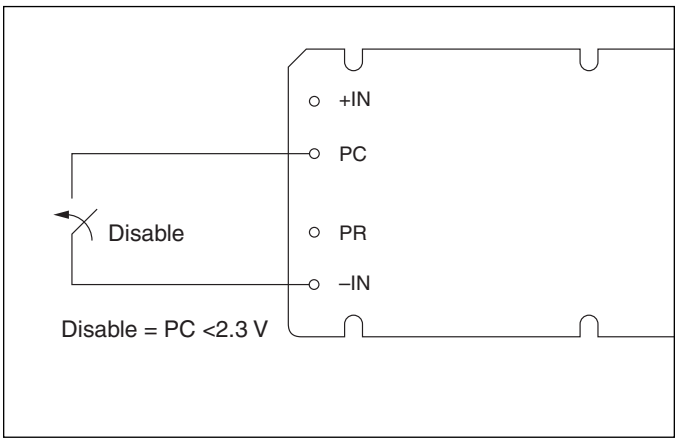


Figure 2–1 *— Module Enable / Disable*

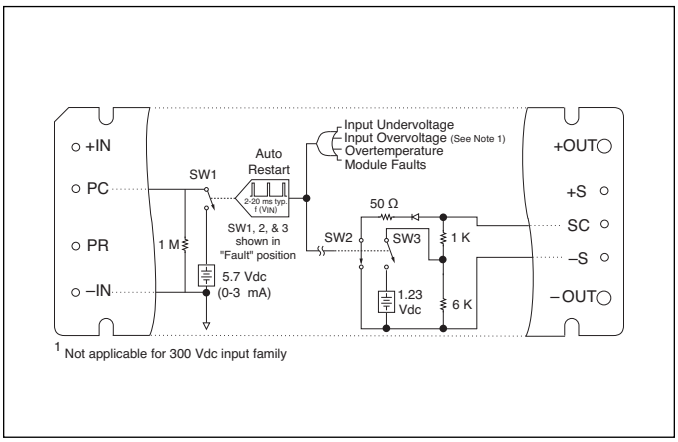


Figure 2–2a *— PC and SC module alarm logic (Maxi / Mini)*

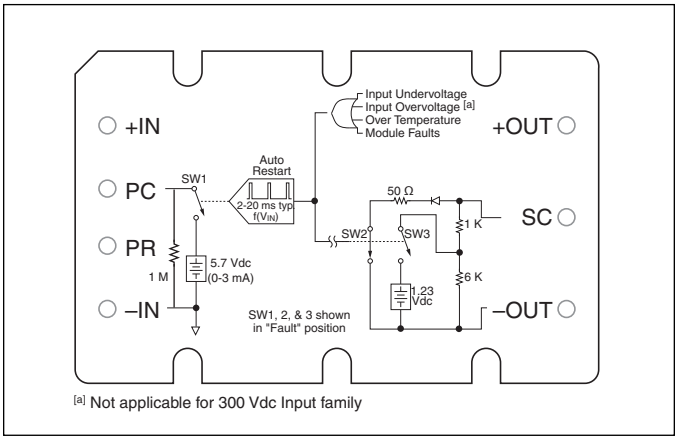


Figure 2–2b *— PC and SC module alarm logic (Micro)*

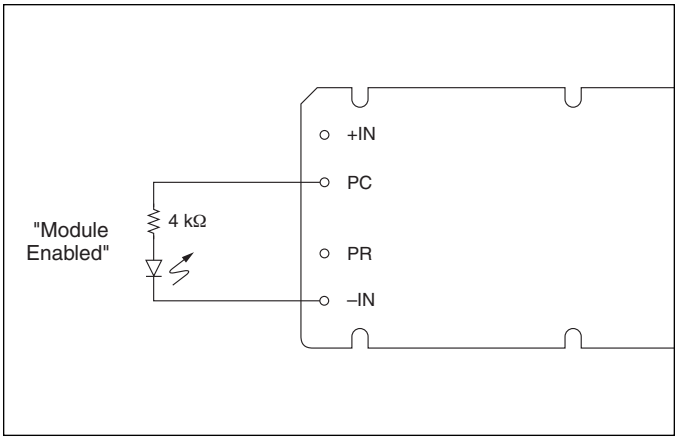


Figure 2–3 *— LED on-state indicator*

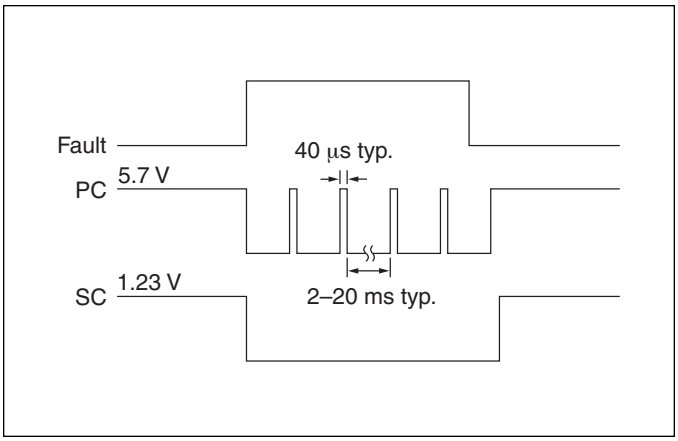


Figure 2–4 *— PC / SC module alarm timing*

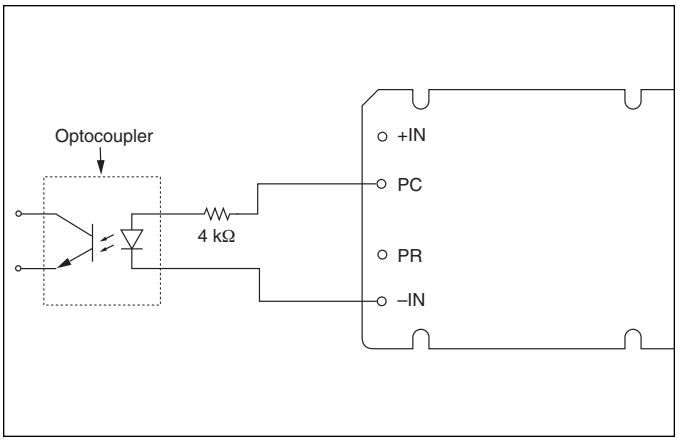


Figure 2–5 *— Isolated on-state indicator*

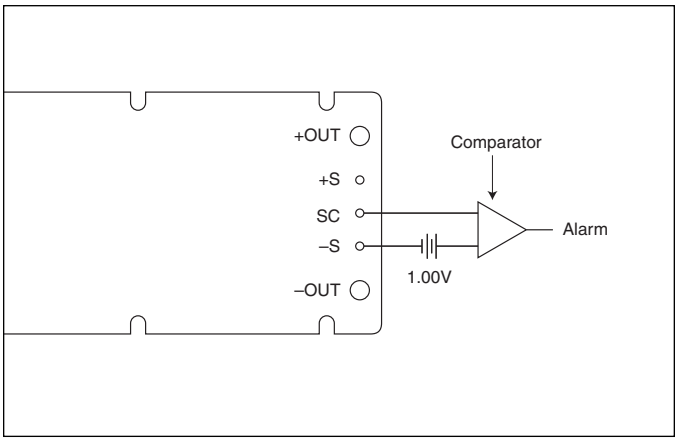


Figure 2–6a *— Secondary side on-state (Maxi / Mini)*

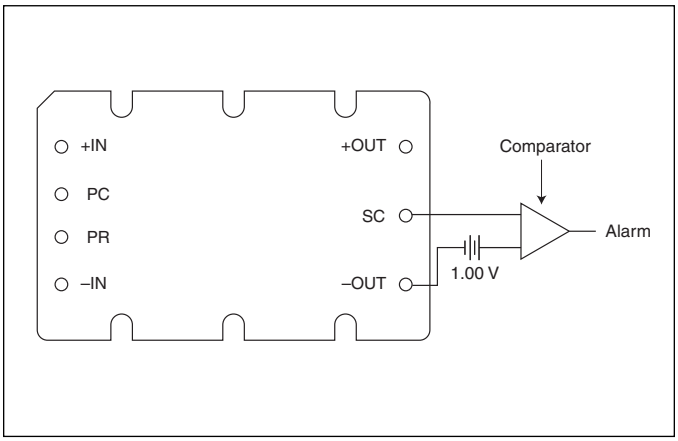


Figure 2–6b *— Secondary side on-state (Micro)*

PARALLEL BUS (PR PIN)

A unique feature has been designed into Vicor Maxi, Mini, Micro converter modules that facilitates parallel operation for power expansion or redundancy. The PR pin is a bi-directional port that transmits and receives information between modules. The pulse signal on the parallel (PR) bus serves to synchronize the high-frequency switching of each converter which in turn forces them to load share. These modules possess the ability to arbitrate the leadership role; i.e., a democratic array. The module that assumes command transmits the sync pulse on the parallel bus while all other modules on the bus listen. In the event of a failure of the lead module, the array "elects" a new leader with no interruption of the output power.

Connection methods for the PR bus include:

1. AC-coupled single-wire interface: All PR pins are connected to a single communication bus through 0.001 µF (500 V) capacitors. This interface supports current sharing and is fault tolerant except for the communication bus. (Figure 2–7) This method may normally be used with a maximum of three converters.
2. Transformer-coupled interface: Modules or arrays of modules may also be interfaced to share a load while providing galvanic isolation between PR pins via a transformer-coupled interface. For large arrays, buffering may be required. The power source for the buffer circuit may be derived from the PC pins. For arrays of four or more modules, the transformer coupled interface is recommended. (Figure 2–8)

PARALLEL OPERATION CONSIDERATIONS

Care must be taken to avoid introducing interfering signals (noise) onto the parallel bus that may prevent proper load sharing between modules, instability, or module failure. One possible source of interference is input ripple current conducted via the + and –Input power pins. The PR signal and DC power input share a common return, which is the –Input pin. Steps should be taken to decouple AC components of input current from the parallel bus. The input to each converter (designated as + and – pins on the input side of the module) should be bypassed locally with a 0.2 µF ceramic or film capacitor. This provides a shunt path for high frequency input ripple current. A Y-rated 4,700 pF capacitor should be connected between both the + and –Input pins and baseplate of each module, thus creating a shunt path for common-mode components of current. Attention to the PC board artwork should minimize the parasitic impedance between –Input pins of parallel modules to ensure that all PR pins are referenced to the same potential, or use a transformer coupled interface. Modules should be placed physically close to each other and wide copper traces (0.75 in./19 mm, 2 oz. copper) should be used to connect power input pins. A dedicated layer of copper is the ideal solution.

Some applications require physical separation of paralleled modules on different boards, and/or input power from separate sources. For applications using separate sources, please refer to the "Hot-Swap Capability Eliminates Downtime" application note on Vicor's website. In these cases, transformer coupling of the PR signal, per Figure 2–8, is required to prevent inter-module common-mode noise from interfering with the sync pulse transmission. High-speed buffering may be required with large arrays or if the distance between modules is greater than a few inches. This is due to the fact that all modules, except the one that's talking, are in the listening mode. Each listener presents a load to the master (talker), which is approximately 500 Ω shunted by 30 pF capacitance. Long leads for the interconnection introduce losses and parasitic reactance on the bus, which can attenuate and distort the sync pulse signal. The bandwidth of the bus must be at least 60 MHz and the signal attenuation less than 2 dB. In most cases, transformer coupling without buffering is adequate. Many applications may benefit from the addition of Z1, in series with the PR Pin of each converter. A low Q 33 Ω @ 100 Mhz ferrite bead or a 5 - 15 Ohm resistor may be used to improve the PR signal waveform. Although this is not a requirement, it can be very helpful during the debug stage of large converter arrays to help improve the PR pulse wave shape and reduce reflections. Again, careful attention must be given to layout considerations. When the outputs of two or more converters are connected in a parallel array to increase system power the converters should be "group enabled" to ensure that all the converters start at the same time. The PC pins of all converters in the array should be controlled by an external circuit which will enable the converters once the input voltage is within the normal operating range. Please consult with Applications Engineering at any Vicor Technical Support Center for additional information.

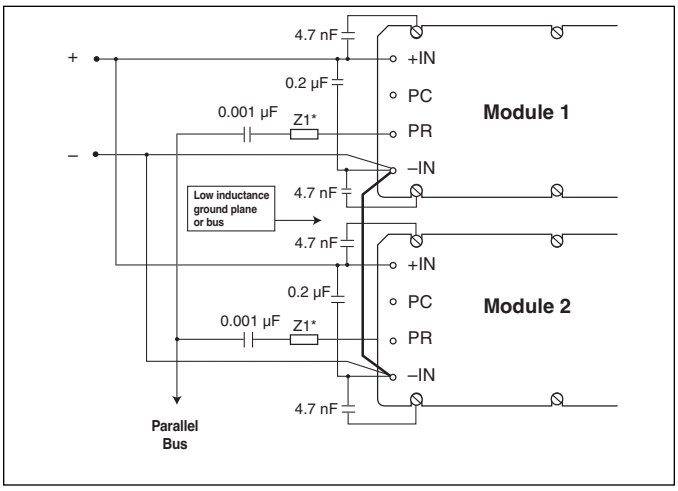


Figure 2–7 *— AC coupled single-wire interface*

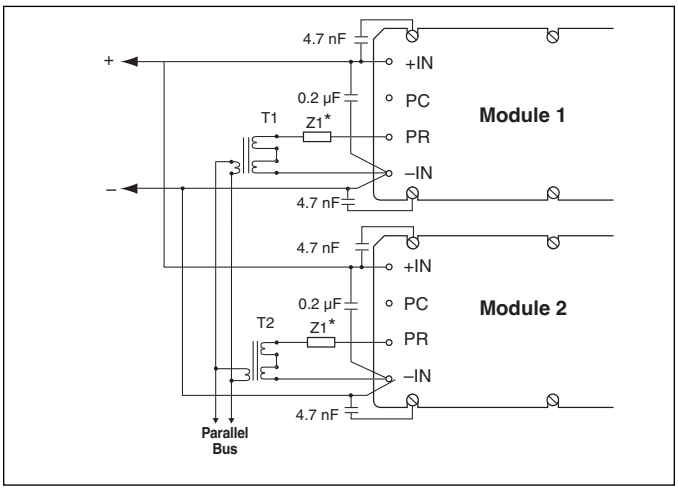


Figure 2–8 *— Transformer-coupled interface*

CONTROL FUNCTIONS AND OUTPUT CONSIDERATIONS

Parallel Operation (PR Pin). The PR pin supports paralleling for increased power with N+1or N+M redundancy. Modules of the same part number will current share if all PR pins are suitably interfaced. Figures 2–9 and 2–10 show connections for the Maxi and Mini modules; Figure 2–11 shows connections for Micro array. Applications containing two or more Micro modules must define a designated master (talker) by stagger trimming the output voltage of each subsequent module down by at least 2%, or setting the remaining Micro modules in the system as designated listeners by connecting the SC pin to the negative output pin.

PR Pin Considerations. When paralleling modules, it is important that the PR signal is communicated to all modules within the parallel array. Modules that do not receive a PR pulse in a parallel array will not current share and may be damaged by running in an over-power condition.

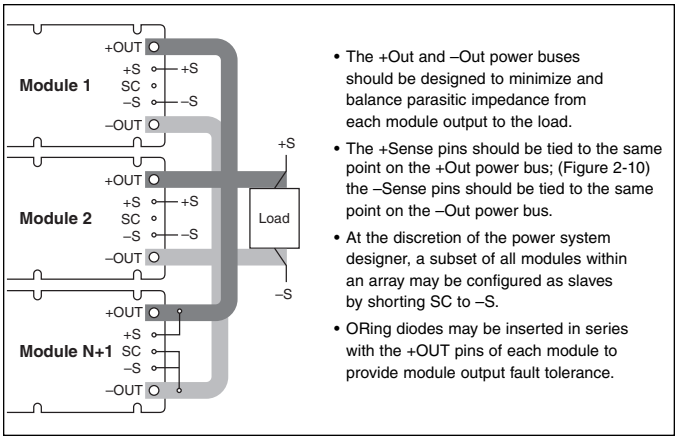


Figure 2–9 *— N+1 module array output connections (Maxi and Mini)*

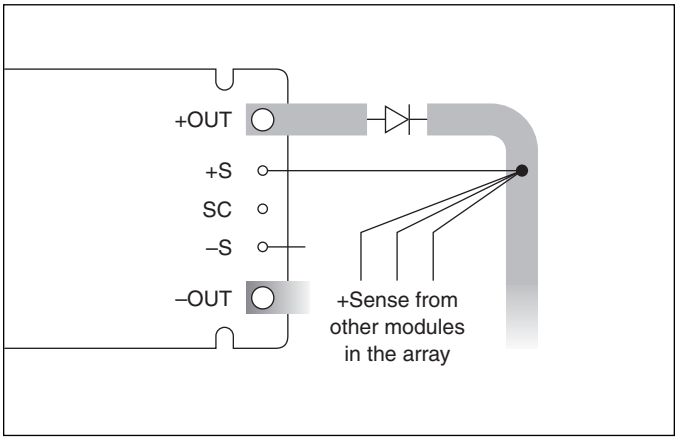


Figure 2–10 *— ORing diodes connections (Maxi and Mini)*

All modules in an array must be of the same part number.Series connection of outputs is accomplished without connecting the PR pins and allowing each module to regulate its own output voltage. Since the same current passes through the output of each module with the series connection, power sharing is inherent. Series connection of inputs requires special precautions, please contact Applications Engineering for assistance.

Array Output Overvoltage Protection (OVP). In order to maintain the highest possible uptime of a parallel array the converters use an output overvoltage protection system (OVP) that is highly resistant to false tripping. For the converter to shut down due to an OVP condition two conditions must be satisfied (logical AND);

1. The voltage at the output terminals must be greater than the OVP set point.
2. The secondary control IC within the converter must be requesting a power conversion cycle from the internal primary control IC.

By using this logic, false tripping of individual converters due to externally induced OVP conditions such as load dumps or, being driven by an external voltage source at the output terminals is minimized.

Modules connected in a parallel array rely on the active master module for OVP of the entire array. Modules acting as boosters (slaves) in the array are receiving external requests for power conversion cycles (PR pulse) and will not shut down from an OVP condition. Therefore it is imperative that the + and -Output pins of modules connected in a parallel array **never** be allowed to become open circuited from the output bus. An open circuit at the output terminals will result in terminal voltages far in excess of the normal rating causing permanent damage to the module and possible hazardous conditions.

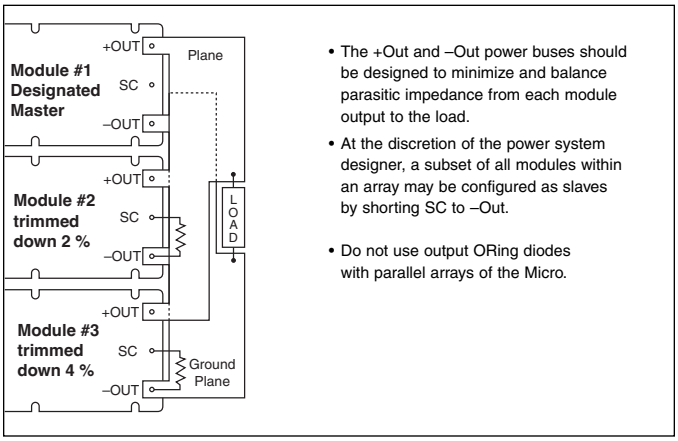


Figure 2–11 *— Parallel module array output connections (Micro)*

CONTROL FUNCTIONS, SECONDARY CONTROL (SC PIN)

Output Voltage Programming. The output voltage of the converter can be adjusted or programmed via fixed resistors, potentiometers or DACs.

Trim Down. The converter is **not** a constant power device; it has a constant current limit. Hence, available output power is reduced by the same percentage that output voltage is trimmed down. Do not exceed maximum rated output current. The trim down resistor must be connected to the –S pin (–Out pin on a Micro). (Figures 2–12a and 2–12b)

Trim Up. The converter is rated for a maximum delivered power. To ensure that maximum rated power is not exceeded, reduce maximum output current requirement in the application by the same percentage increase in output voltage. The trim up resistor must be connected to the +S pin (+OUT pin on a Micro.) Do not trim the converter above maximum trim range (+10%) or the output over voltage protection circuitry may be activated. (Figures 2–13a and 2–13b)

SC Pin and Output Voltage Trimming. If no connection is made to the SC pin, the SC pin voltage will be 1.23 V referenced to –S (-OUT pin on a Micro) and the output of the converter will equal the nominal output voltage. When the SC pin voltage is set by an external source such as a D/A converter, the % change in SC will be equal the % change in the output voltage.

For example, an application requires a +10, 0% (nominal), and a –15% output voltage adjustment for a 48 V output converter. Referring to the table below, the voltage that should be applied to the SC pin would be as follows:

V_{SC}	V_{OUT}	Change from nominal
1.046	40.8	–15%
1.230	48.0	0%
1.353	52.8	+10%

Circuits such as op-amps and D/A converters, which directly drive the SC pin, should be designed to limit the applied voltage to the SC pin. It is also important to consider voltage excursions that may occur during initialization of the external circuitry. The external circuit must be referenced to the –S pin (–Out on Micro). See Figure 2–14 for remote sense implementation on Micro.

For systems that require an adjustable output voltage, it is good practice to limit the adjustment range to a value only slightly greater than that required. This will increase the adjustment resolution while reducing noise pickup.

It is recommended that the maximum rate of change applied to the SC pin be limited to 30 Hz, sinusoidal. Small step-up changes are permissible; however, the resultant change in the output voltage can create significant current demands due to charge requirements of both the internal and external output capacitance. In no case should the converter be driven beyond rated continuous output current. The response to programming a lower output voltage is limited by the energy stored in both the internal and external output capacitance and the load. The converter cannot sink current to lower the output voltage other than a minimal internal preload.

Contact Applications Engineering if the module's output is to be dynamically trimmed.

Trimming resistor calculators are available on Vicor's web site at www.vicorpower.com/tools. (Figure 2–16)

Resistor values can be calculated for fixed trim up, fixed trim down, and for variable trim up or down. In addition to trimming information, the web also includes design tips, applications circuits, EMC suggestions, thermal design guidelines and PDF data sheets for all Vicor products. Evaluation Boards (Figure 2–15) are available for the Maxi, Mini and Micro DC-DC converters.

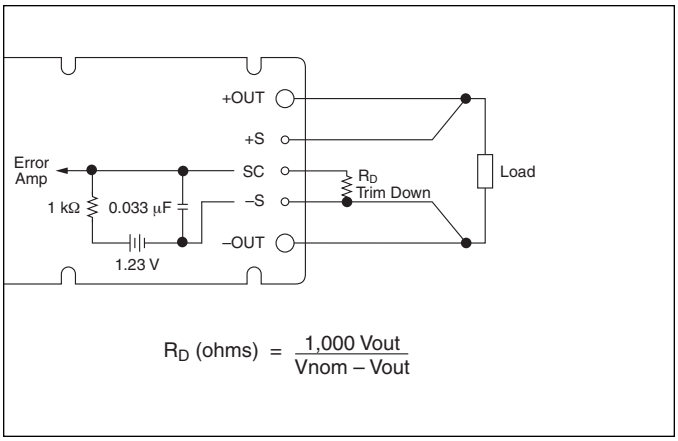


Figure 2–12a *— Output voltage trim down circuit (Maxi / Mini)*

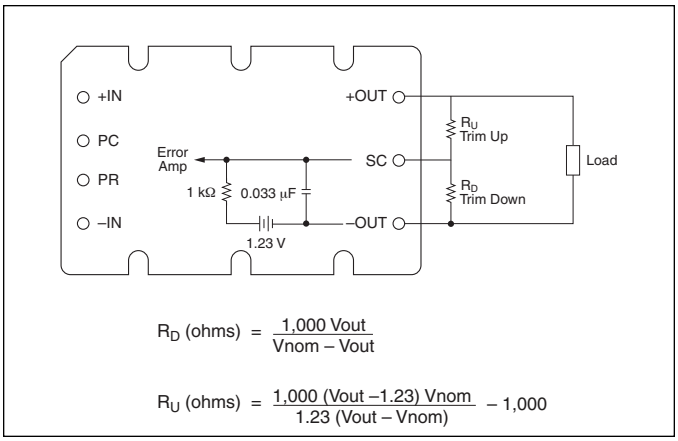


Figure 2–12b *— Output voltage trim down circuit (Micro)*

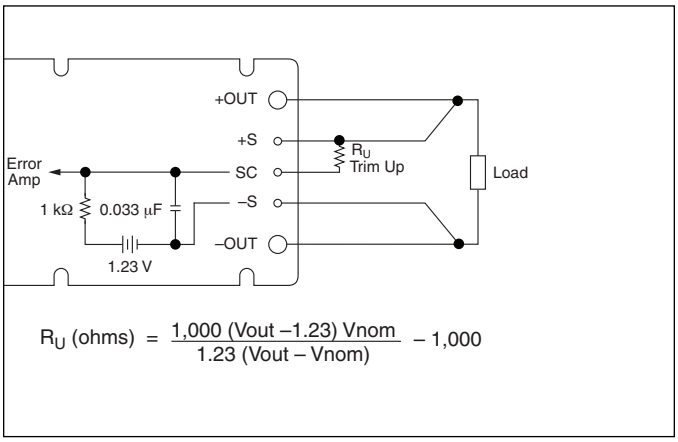


Figure 2–13a *— Output voltage trim up circuit (Maxi / Mini)*

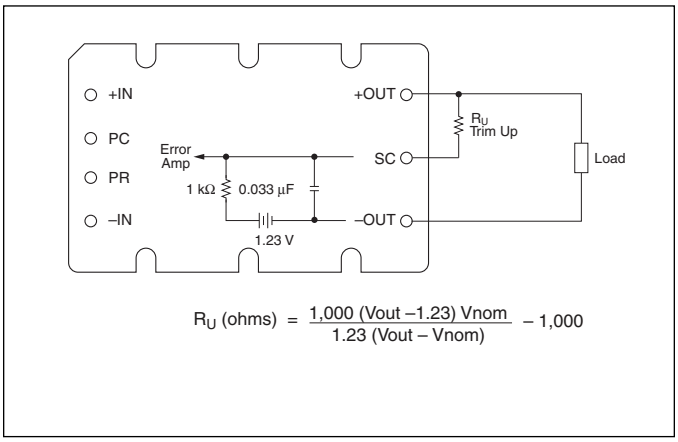
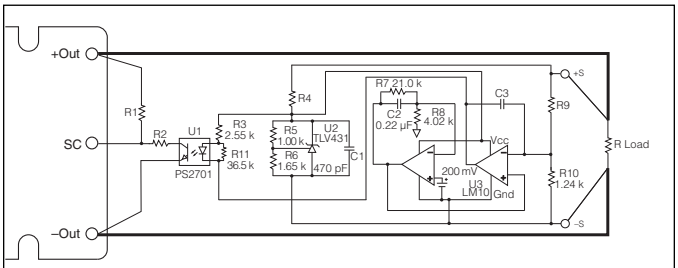


Figure 2–13b *— Output voltage trim up circuit (Micro)*



- This module is designed for point of load regulation, where remote sensing is not required. Active voltage drop compensator, as shown here, may be used in applications with significant distribution losses.

  Please consult with the Micro Family Isolated Remote Sense Application Note for additional information.

Figure 2–14 *— Voltage drop compensation (Micro).*

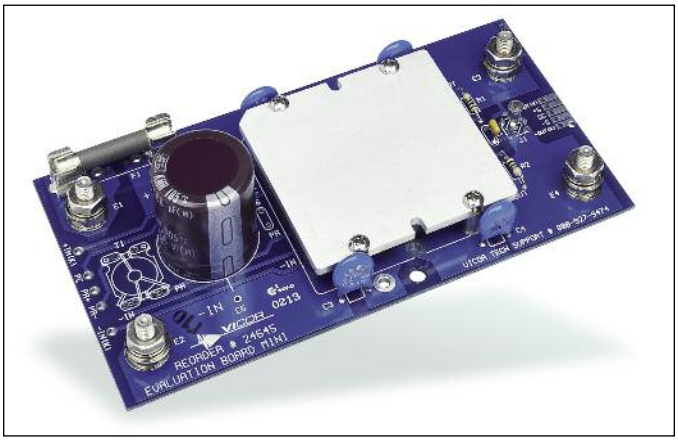


Figure 2–15 *— Evaluation Boards; Available for Maxi, Mini and Micro Family DC-DC converters*

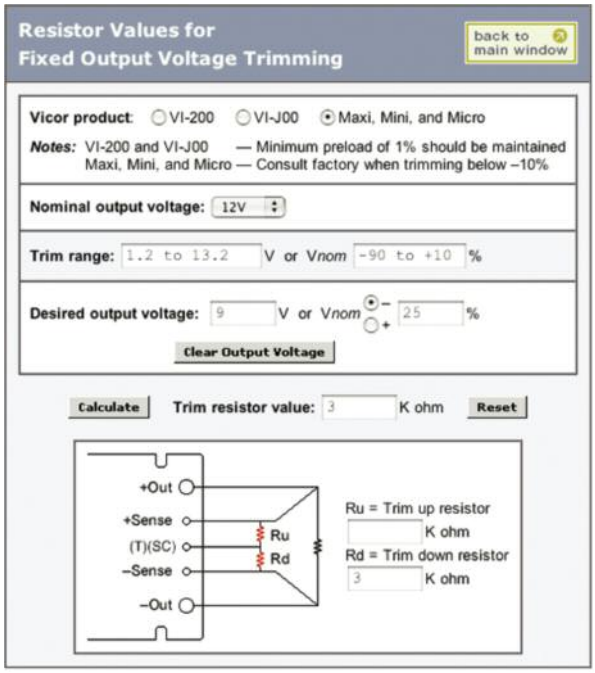


Figure 2–16 *— Online trim calculator*

EVALUATION BOARDS

- Three styles: Maxi, Mini or Micro
- Short pin and Long pin compatible
- Easy I/O and control connections
- Includes fusing and capacitors
- Can be paralleled for higher power arrays

DESCRIPTION	PART NUMBER
Maxi board style	24644R
Mini board style	24645R
Micro board style	24646R